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MISSILE MANUFACTURING TECHNOLOGY CONFERENCE HELD AT HILTON HEAD ISLAND, SOUTH CAROLINA ON 22-26 SEPTEMBER 1975. PANEL PRESENTATIONS. TEST EQUIPMENT

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POTENTIAL REFINEMENTS AND INNOVATIONS
IN AUTOMATIC INSPECTION AND TEST TECHNIQUES

R. K. Gundal
J. F. King
S. J. Ring

Raytheon Company

Andover, Mass. 01810

ABSTRACT

This paper will describe the evolution of the Improved HAWK and SAM-D automatic test systems in use at Raytheon's West Andover Massachusetts facility, and will develop projects which will continue the evolutionary process toward more cost effective test systems employing the most current technology.

IMPROVED HAWK TEST SYSTEM

The Improved HAWK automatic test system was conceived and implemented in the period 1967 - 1969. The driving force for a highly sophisticated and versatile automatic test system was conversion of the HAWK missile system from the tube technology of the 1950's to the solid state technology of the 1960's. With this conversion and the advent of a digital computer in the ground support equipment came a relatively high volume of many types of modules to be tested.

In the early-to-mid 1960's, the minicomputer was making it's presence felt in the electronics field, but was still comparatively expensive. These facts, coupled with the high cost of computer peripherals and the problems relative to system management, drove Raytheon to the test system configuration shown in Figure 1 which was initially installed with approximately 20 test stations on-line.

The test stations, which were part of this initial configuration, shared the same basic structure shown in Figure 2 and consisted of the following types:

<u>Ground Support Stations</u>

(1) Pulse Analog Modules
(2) Digital Modules
(3) Analog Modules
(4) D.C. and Synchro Modules

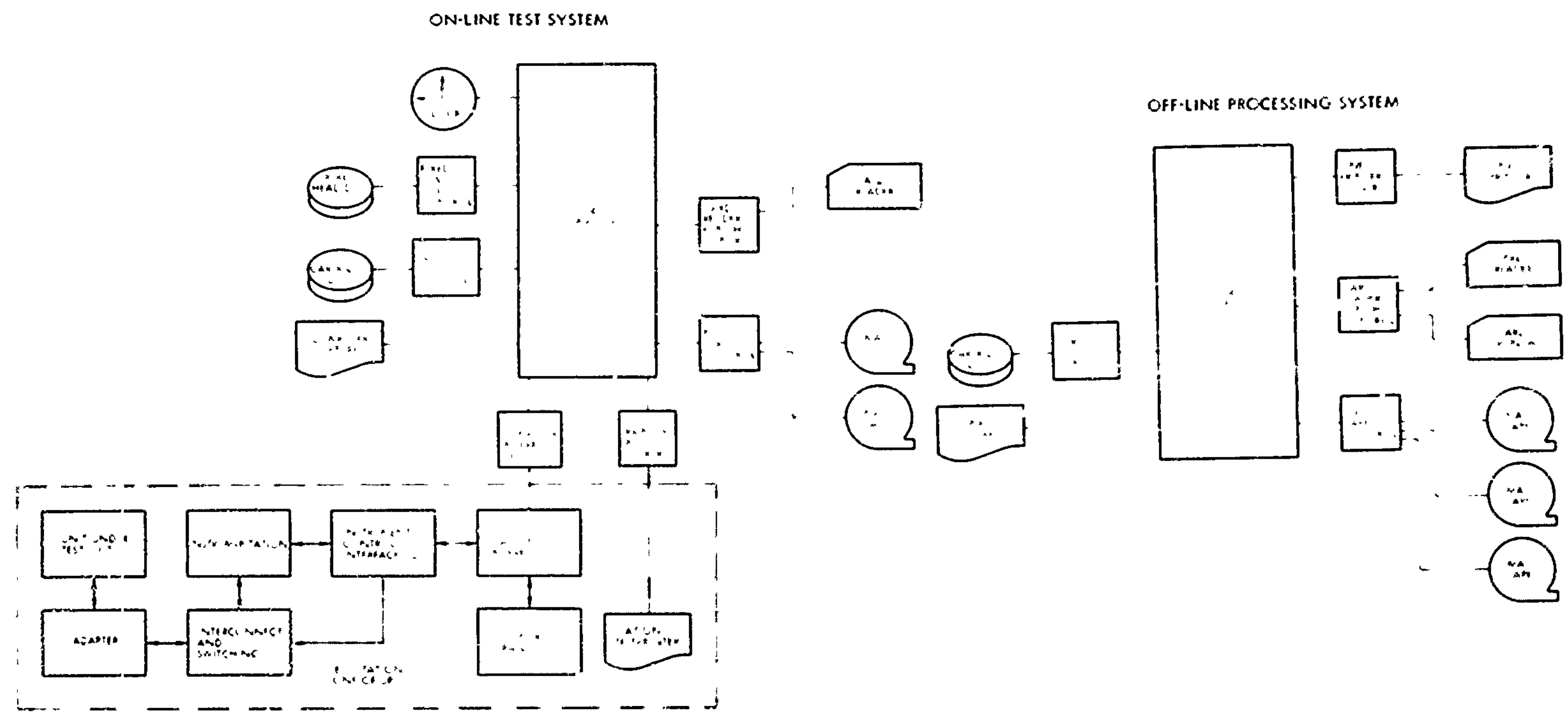

ON-LINE TEST SYSTEM
OFF-LINE PROCESSING SYSTEM
ADAPTER
INTERCONNECT AND SWITCHING

FIGURE 1

IH TEST STATION GENERAL BLOCK DIAGRAM

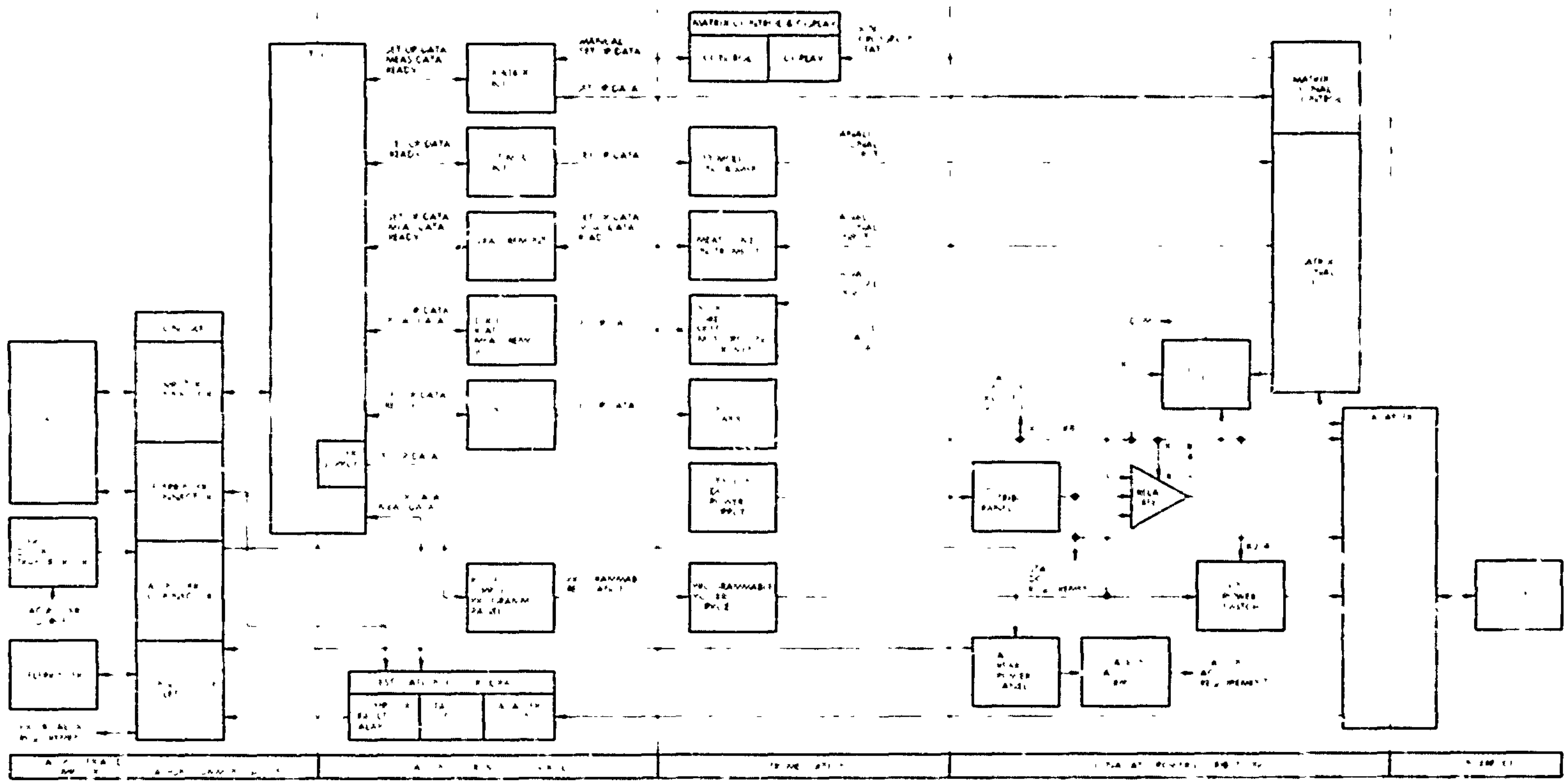


FIGURE 2

Missile Stations

(1) High Frequency Modules
(2) Low Frequency Modules
(3) Stick (Chassis) Stations (3 types)
(4) Hydraulic Actuator

Microwave Stations

(1) Randome Test
(2) Antenna Test (2 types)
(3) Microwave Component
(4) Microwave Subsystem

Although these station types are dedicated to vastly different ends, they are all comprised of the same basic components and constructed from the same basic architecture.

This system (which is described in detail in Appendix A) is now operating with approximately 50 production test stations at Raytheon's West Andover facility, and has recently been deployed in three European locations in support of the NATO HAWK program.

SAM-D TEST SYSTEM

The SAM-D Automatic Factory test system, put into operation in 1973, was an evolution of the Improved HAWK Automatic Factory Test System. The SAM-D system is a multi-computer distributive intelligence test system organized around a central computer with extensive mass memory and other peripherals. This central computer is time shared by up to 32 satellite computers, each of which is the resident real-time process controller in an automatic test station. All software, such as a monitor, an editor, a compiler, a loader, an operating system, test programs, and diagnostics are available from the central computer library to be run in real-time on the station process controllers. A test station operator interface terminal consisting of a CRT display, keyboard, and printer permits the preparation, editing, debugging, and execution of programs to occur simultaneously at each test station. The system architecture still retains the advantages of centralized electro-mechanical peripherals and configuration management.

The communication between the central computer and its many satellite test station process controllers is accomplished with a high speed (50,000 16 bit words/second) serial interface system designed to appear as a DMA (Direct Memory Access) peripheral on each computer. The organization of the SAM-D Automatic Factory Test System is more completely described in Figure 3 and Appendix B.

Each test station is configured from standard building blocks that are designed to fulfill those functions which more than one station type has in common. In most cases, these are refinements of the building blocks of the Improved HAWK system, redesigned to incorporate state-of-the-art components, reduce space requirements, and improve maintainability. Thus, the computer, instruments, control systems, power systems, enclosures/racks, and operator interface designs are standardized.

The significant improvements achieved by the SAM-D test system architecture, as it evolved from the Improved HAWK test system base of experience, are as follows:

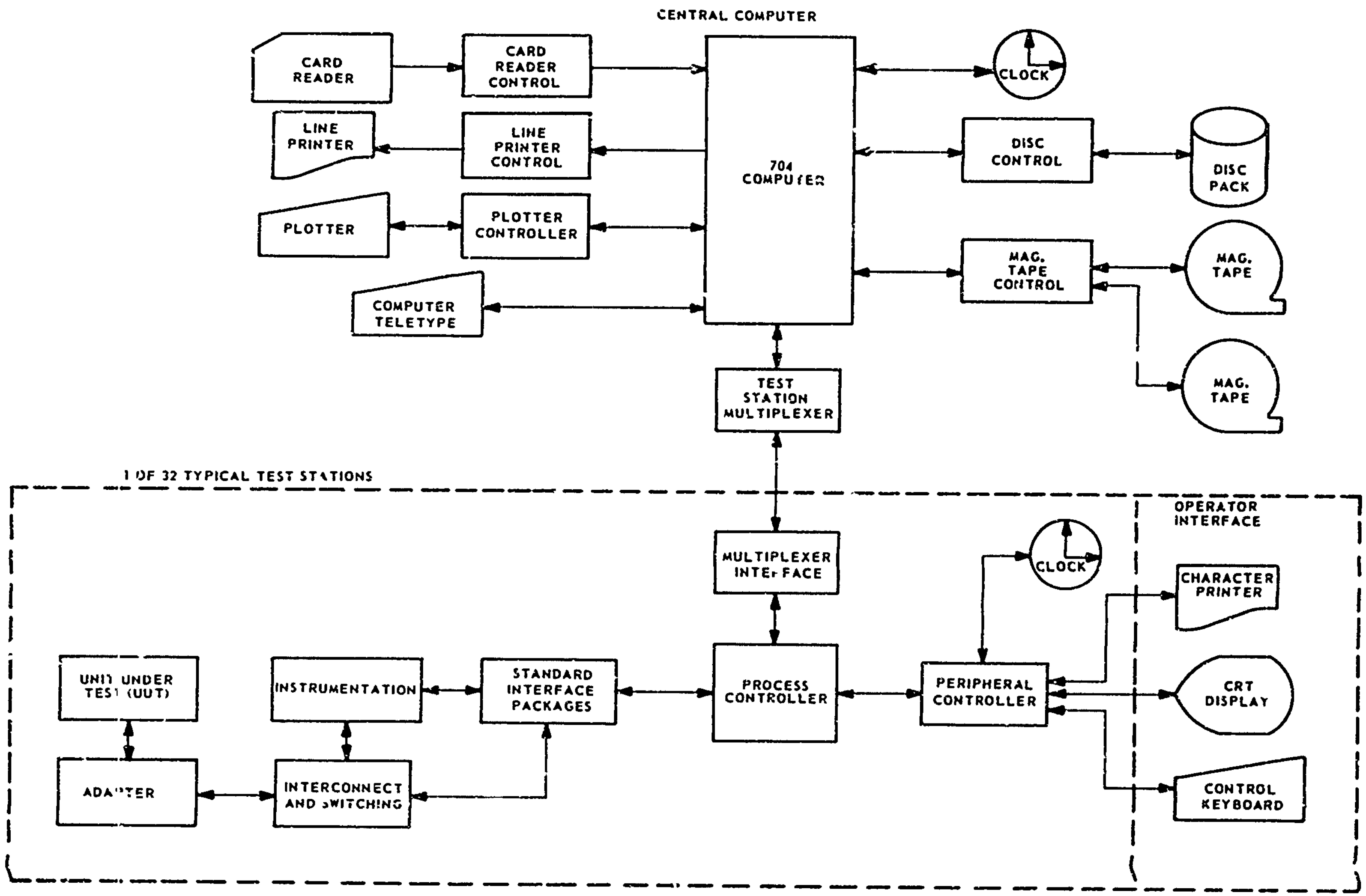


Figure 3 SAM-D FACTORY TEST SYSTEM BLOCK DIAGRAM

TEST EQUIPMENT COST ELEMENTS (percent)

	MAT'L	PURCHASED PARTS	FABRICATION	ASSEMBLY	TEST AND INSP.	SUPPORT	DEVELOPMENT	% PRODUCTION COST
Commercial Instruments		92		1	2		5	11
Data Processors		79		1	1	4	15	7
Switching Networks		45		9	1	11	34	5
Adapters/Fixtures	3	29	1	17	1	22	27	18
Control Systems	1	41	3	5	1	12	37	5
Enclosures/Racks		20	37	12			31	2
Environmental Cont.		55		12			33	1
Power Supplies	1	28	9	33	7	7	15	4
Cables & Harnesses	2	6		21	7	13	46	6
Executive Software							100	6
UUT Software						37	63	16
Documentation							100	17
Special Panels & Displays	1	61	4	13	3	7	11	1

FIGURE 4

(1) A CRT display and keyboard which permits extensive and efficient man-machine interaction.

(2) An on-line compiler and editor which permits program development to occur at each test station with the results of any changes able to be evaluated "on-the-spot".

(3) Improved diagnostics which allow the maintenance technician to communicate with the test station instrumentation in source-like language statements by means of the CRT display and keyboard.

(4) An improved high level language with additional features such as statements to facilitate writing programs to test digital devices.

(5) Larger and faster mass memory available at the central computer.

(6) Real-time program execution which results in repeatable timing and more independence from the central computer.

(7) Double the number of satellite test stations which can be served by one central computer.

The manufacturing technology projects which are defined here-in are evolved from the experience gained in the design, development, and day-to-day usage of the two automatic test systems which we have mentioned.

These projects do not necessarily focus on drivers for the recurring costs of test equipment (see Figure 4), but could result in the reduction of non-recurring development costs and increased equipment utilization. It is these latter areas which are most likely to yield significant test related cost reduction over the life of any given missile program.

MISSILE MANUFACTURING TECHNOLOGY PROJECTS

Automatic Part Identification

Title: Manufacturing Technology Project to provide a system for the automatic reading and recording of part and serial number information of units tested on automatic equipment.

System/Panel Area/Component: HAWK - SAM-D/test equipment/control system

Problem: In the utilization of sophisticated automatic test equipment for high volume multi-unit testing of missile system hardware, it is necessary to supply the controlling computer with the part number (to obtain the correct programs) and serial number (to identify retained data and control configuration). Existing schemes for supplying this information are either to dial the information into thumbwheel switches or key the information into a keyboard (teleprinter or other).

Both of these systems are relatively slow, and are subject to a high incidence of operator error.

Proposed Solution: This project would investigate alternate methods for capturing this information in a more automated fashion using punched identification cards, or bar coding techniques such as are employed in retail stores

Project Cost and Duration: Estimated costs are as follows:

Engineering development and documentation	$140,000
Prototype material and fabrication	100,000
	$240,000

Estimated duration of project is 12-15 months.

Benefits: Benefits to be derived from this project are the reduction in the unit set up time for test, and the reduction in errors made in acquiring part identification information.

Potential Cost Savings - 1% of Missile test time
1% of Ground Equipment MI (Major Item) test time

Assumption: This project has application only to a high volume production environment.

Automatic Fault Isolation Techniques

Title: Manufacturing Technology Project to develop automatic fault isolation techniques.

System/Panel Area/Component: HAWK - SAM-D/test equipment/NA

Problem: When using automatic test equipment for the high volume testing of missile system hardware, troubleshooting and fault isolation becomes a significant problem. It is normally not feasible to provide an off-line facility for this purpose and therefore, the expensive and highly productive automatic equipment is used for troubleshooting.

Solution: Investigate alternate methods of fault isolation which would use the automatic test equipment more efficiently. Some of the techniques which would be investigated are as follows:

(1) The use of infra-red scanning techniques to generate and store the thermal profiles of known good units which may then be compared with the thermal profile of failed units. The resulting difference data may then be used as an aid in fault isolation.

(2) Techniques for capturing and storing the signal levels for all internal nodes at each step in the test sequence of a good unit. Also develop suitable methods for presenting this information to a test operator while troubleshooting a bad unit.

(3) The development of techniques to aid in the fault diagnosis of digital devices utilizing the input/output fault signature of the failed unit in conjunction with computer aided analysis.

Project Cost and Duration: Estimated costs are as follows:

Engineering development and documentation	650,000
Prototype material and fabrication	400,000
	1,050,000

Estimated duration of project is 18 months.

Benefits: The benefit which will be derived from this project is to increase the throughput of automatic test equipment by reducing troubleshooting time and erroneous fault diagnosis.

Potential Cost Savings - 10% of Missile Test Time
10% of Ground Equipment MI test time

Assumptions: The benefit will only be obtained if the existing philosophy is to use the automatic test equipment for test and troubleshooting, and that the applicable programs have sufficient volume to warrant the investment.

Standard Building Blocks

Title: Manufacturing Technology Project to develop standard building blocks for factory and field test equipment of common architecture.

System/Panel Area/Component: SAM-D/test equipment/control systems, data processors, switching networks, special panels/displays, executive software, and UUT software.

Problem: Automatic test equipment incurs a high development cost due to its complexity and extensive software development effort. This high cost relegates its use to high volume manufacture. Therefore, the many benefits of automation; reduced test time, repeatability, data collection, data analysis, efficiency, accuracy, machine aided troubleshooting, and others are not available to low volume complex electronic assemblies in the factory or to the low quantity/large variety mix of the field.

Proposed Solution: Develop a test system tailored to module and chassis level of military electronics systems, applicable to the factory and depot level. Typical activities would include:

(1) High level instrument control oriented test language, compiler and operating system compatible with different assembly languages.

(2) A standard building block for test station controller (processor and operator interface).

(3) Switching networks standard building blocks.

(4) Instrument interface standard building blocks.

(5) Digital pin(s) electronics module standard building block.

Project Cost and Duration: Estimated costs are as follows:

Engineering labor and documentation	1,025,000
Prototype material and fabrication	320,000
	1,345,000

Estimated duration of project is 18 months.

Benefits: The benefits that accrue from this project are lower automatic test equipment development costs through the use of standard building blocks of hardware and software which can be assembled into test stations configured to accomplish a unique group of related functions. Additional task specific benefits are detailed below:

(1) The high level computer language task will accrue the following benefits:

(a) Provide a standard building block for automated test equipment potentially common to laboratory, factory, and field.

(b) Enable the power of the RATEL instrument control oriented language to be used more universally.

(c) Simplify the design and use of microprocessor based test equipment by providing the capability of programming in a proven test instrumentation oriented high level language.

(d) Lower the software development and support costs of automatic test equipment based on computers or processors other than Raytheon 700 series minicomputers.

(e) Potential Savings - 40% of Executive software Development Cost
80% of UUT Program Development Cost

(2) The standard controller and operator interface task will accrue the following benefits:

(a) Provide a standard building block for automated test equipment potentially common to the laboratory, factory, and field.

(b) Provide a standardized operator interface which is independent of test station configuration whether it be testing DC power supplies or microwave components.

(c) Station control, data gathering, and housekeeping functions, both hardware and software, are standard "off-the-shelf" and low in cost.

(d) Minimize test station console space requirements for automation hardware.

(e) Potential Savings - 90% of Test Station Process Controller Development Cost

(3) The standard switching networks task will accrue the following benefits:

(a) Provide standard building blocks for automated test equipment potentially common to laboratory, factory, and field.

(b) Reduce cost of switching which is presently vendor special and station unique.

(c) Permit standardization of software and display relative to switching functions thus lowering housekeeping software and training requirements of new personnel assigned to test station operation or maintenance.

(d) Potential Savings - 50% of Test Station Switching System Development Cost

(4) The standard instrument interface task will accrue the following benefits:

(a) Provide standard building blocks for automated test equipment potentially common to laboratory, factory and field.

(b) Reduce cost of instrument interfaces by reducing number of unique designs, thus, lowering documentation, troubleshooting training, and spares stocking requirements.

(c) Potential Savings - 50% of Test Station Control System Development Cost

(5) The pin(s) electronics module task will accrue the following benefits:

(a) Provide a standard building block for digital test equipment which is potentially common to laboratory, factory, and field.

(b) Provide larger memory (greater than 1000 bits), dynamic I/O control, and high speed to facilitate dynamic troubleshooting by furnishing the capability of looping on large, self-initializing test pattern sequences. This feature would provide the capability of probing internal states with a synchronized oscilloscope.

(c) Lower digital test station development and recurring build costs with standard building block.

(d) Increase flexibility of test station configuration by providing fully programmable pin(s) electronics which can be combined in variable quantities with other equipment to meet specific testing needs.

(e) Increase speed of testing by reducing package size, capacitance, and signal line lengths.

(f) Utilize higher density MSI and LSI technology.

(g) Potential Savings - 25% of Digital Test Station Development Cost
5% of Digital Test Station Build Cost

<u>Assumptions</u>: These tasks are based on an evolution of an existing automated test system which has already achieved a high degree of modularity and hardware standardization. The tasks also assume a mature modular software architecture and a proven high level test language.

High Density Interconnecting Network Testing

<u>Title</u>: Manufacturing Technology project to develop techniques for handling and testing high density interconnecting networks.

<u>System/Panel Area/Component</u>: SAM-D/test equipment/fixtures-adapters.

<u>Problem</u>: Interconnecting networks, such as thick-film multilayer ceramic substrates and small dense multilayer printed circuit boards, which have a high density of component interface points are difficult to test. High densities, such as .004 inch pads .008 inch on center, render probing and complete testing for continuity and leakage impractical using presently available techniques. However, the removal of components at the next higher level of assembly is often a destructive process. Therefore, testing at the network level is necessary to minimize the scrapping of good integrated

circuits and other expensive components which were assembled to a bad network.

Proposed Solution: Develop fixturing techniques to make connection to high density interconnecting networks and test them for continuity and leakage. Investigate both a mass probing technioue and a programmably positioned probe pair technique. The mass probe would effect connection to all component interface points simultaneously and then utilize an automatic continuity and leakage test station with enough capability to 100% test the network. The programmably positioned probe pair would position two probes by computer control to locate and effect connection to two points of the network under test. The test station would then perform a continuity or leakage measurement as required. The sequence would be repeated as often as required to test all runs for continuity and all hazardous (adjacent or crossed over) run pairs for leakage.

Project Cost and Duration:

Engineering development and documentation	160,000
Prototype fabrication	40,000
	200,000

The duration of this project is expected to be 15 months.

Benefits:

(1) Increased yield at the next higher level of assembly.

(2) Eliminate scrap caused by destructively removing assembled good components from a defective network.

(3) Eliminate unnecessary and futile troubleshooting and rework of assemblies containing a defective network.

(4) Potential Savings - 2% of Ground Equipment Standard Module Cost

Assumptions: Availability of an automatic continuity and leakage tester large enough to accomodate a mass probed substrate. The computer portion of this test station must be capable of being interfaced to a set of X-Y positioners and the software flexible enough to allow programmed control of these positioners. The test system is assumed to be available on a non-interferring rent free loan basis.

Beam Lead Device Handling and Testing

Title; Manufacturing Technology Project to develop techniques for handling beam leaded integrated circuits.

System/Panel Area/Component: SAM-D/test equipment/adapters-fixtures

Problem: Beam leaded integrated circuits (BLIC's) are complex electronic circuits produced on a single silicon chip with a large number of delicate input/output leads. Assembly of untested BLIC's increases the probability of introducing a defective BLIC to the next higher level of assembly. Good BLIC's may be destroyed, or substrates damaged, in troubleshooting, isolating the faulty component, and reworking the defective assembly. Therefore, testing at the BLIC level is very desireable. Reliable, efficient, low-capacitance and non-destructive techniques for effecting connections between

the many I/O ports of the BLIC and suitable test equipment are not yet available.

Proposed Solution: Develop the capability to fixture, make connection to, and test beam leaded integrated circuits having a large number of I/O pins. Two methods would be investigated:

(1) Handling and testing in a carrier.

(2) Handling and testing from a tacky coated glass slide.

Project Cost and Duration:

Engineering development and documentation	160,000
Prototype fabrication	40,000
	200,000

The duration of the project is expected to be 15 months.

Benefits:

(1) Improved yield at the next higher level of assembly.

(2) Minimization of damaging rework at next higher level of assembly.

(3) Reduced troubleshooting at the next higher level of assembly.

(4) Potential Savings - 2% of Ground Equipment Standard Module Cost

Assumptions: Automatic test equipment which is capable of performing dynamic functional tests (pattern test at speed) and DC parametric tests is available to demonstrate the performance of the developed fixtures/carriers on a non-interferring rent free loan basis.

Automated Printed Wiring Board Inspection

Title: Manufacturing Technology project to develop computer supported automatic inspection system for the inspection of printed wiring boards and assemblies.

System/Panel Area/Component: HAWK - SAM-D/test equipment/NA

Problem: The general practice in industry today is to visually inspect printed circuit boards and printed circuit board assemblies for workmanship and assembly type faults. Since this inspection is a rather routine task, it is very much subject to operator fatigue. Therefore, the probability that defective units will proceed to the next operation and eventually to test is relatively high.

Proposed Solution: Develop a computer supported system which could scan the surface(s) of a printed circuit board (or printed circuit board assembly) using videcon or possibly X-ray techniques. The results of this scan would then be digitized and fed to a computer where the data would be compared with a stored, acceptable pattern for the particular device.

Project Cost and Duration: Estimated costs are as follows:

Engineering development and documentation	300,000
Prototype material and fabrication	200,000
	500,000

Estimated duration of project is 20 months.

Benefits: Benefits to be derived from the project are the reduction in inspection manpower, a potential reduction in inspection time, but most significant a near elimination of inspection errors.

Potential Savings - 50% of Printed Wiring Board Inspection Time

Near Field Antenna Testing

Title: Manufacturing Technology Project to provide a means of making near-field radiation measurements on large antennas.

System/Panel Area/Component: SAM-D/test equipment/NA

Problem: A need exists to make antenna measurements of large antennas indoors. This need is present because of expensive material handling equipment required to lift large antennas to test sites which are generally high above ground level, the large cost of real estate for long outdoor ranges, and the down-time due to weather on all outdoor ranges. An indoor configuration would minimize the requirement for handling equipment and the amount of real estate needed, and would eliminate any station down-time due to weather.

Proposed Solution: The project would be split up into two phases. First, a study would be made to identify and analyze the tradeoffs required to select the best possible test methods. At present, two methods are available for investigation, however, this does not eliminate other methods which may come to light during the study. The first of these methods would refocus the energy impinging on the antenna under test to the transmitting antennas which would be located at a distance of several aperture diameters away from the antenna under test. Once this was done, antenna patterns would be taken as on any long antenna range. The second method would be to probe the near-field of the antenna very accurately, then use this data to synthesize the far-field pattern of the antenna. While the first method would be more straight-forward and less complex, it is applicable only on antennas which have complete phase control over the aperture - namely a phased array. The second method would be applicable for any antenna.

Project Cost and Duration:

Engineering development and documentation	125,000
Prototype material and fabrication	250,000
	375,000

Estimated duration of the project is 18 months.

Benefits: The overall benefits from this type of test system are as follows:

(1) No production down time due to weather.

(2) Minimal real estate required.

(3) Minimal handling equipment required.

(4) Lends itself to automatic testing thus cutting down test time and increasing accuracy.

APPENDIX A (1)

1.2 SYSTEM STRUCTURE

1.2.1 Hardware Structure

1.2.1.1 General. The Improved HAWK Factory Test Computer System is an automatic test system composed of a central computer and peripherals which are time shared between from 1 to 16 remotely located test stations. These stations share a modular organization consisting of a standard Test Station Interface (TSI), a standard Test Station Control Panel, and a group of Instrument Control Interfaces (ICI's). The balance of each test station is function dependent and can be as different, station to station as are the available measurement and stimuli instrumenation. The control of this instrumentation is accomodated by the ICI and associated software driver designs. The resulting test system satisfies the following system objectives:

Maximizes test station throughput.

Minimizes operator intervention and decision making.

Provides the ability to test virtually any type of electrical or electromechanical UUT (Unit Under Test) covering the frequency spectrum from DC to X-band.

Provides the ability to construct and maintain test data files with fast recall capabilities.

Maximizes system availability.

Minimizes programming knowledge required in the preparation of UUT programs.

Provides a flexible and modular system with building block type expansion capabilities to accomodate future testing requirements.

Minimizes cost of construction and system maintenance.

To achieve these objectives, the Computer System performs the following functions and/or tasks:

a. Control

(1) Provides automatic control of all programmable stimuli, measurement instrumentation, and interconnection switching networks within the various test stations.

(2) Provides, in programmed sequence, the digital control information required by a test station to perform a UUT test.

b. Data Handling

(1) Accepts measurement data from the test station instrumentation for each test performed.

(2) Accepts input data from the test station operator such as that information which identifies the part being tested and those decisions resulting from visual observation and interpretation.

(3) Interprets test data and makes decisions as to its validity, conformance and acceptability.

(4) Implements automatic chronological data collection including time and date of data receipt and provides immediate or delayed access to this data or a summary of test results.

(5) Organizes test data from each UUT into common format and units and collects this data on IBM compatible magnetic tape. It performs any data conversion required, maintains test histories, and provides limited statistical analysis of the test results.

c. Diagnostics

(1) Provide continual monitoring and confidence testing of data transmissions, critical station parameters, and UUT stimuli.

(2) Provide programmed aids to maintenance personnel to assist them in ascertaining the health of the test system and diagnosing failures to the lowest level possible.

d. Library Maintenance

(1) Provides off-line compilation and debug of UUT test programs to generate object programs.

(2) Provides means of introducing, maintaining, and updating UUT program files and provides the test station with accessibility to these programs.

To achieve the system objectives, the test station performs the following tasks:

a. Interfaces the UUT to the test instrumentation.

b. Provides accurate power, stimuli, and other inputs to the UUT as required by the Test Requirements Specifications (TRS).

c. Provides loads to the outputs of the UUT as required by the TRS.

d. Makes accurate measurements of the outputs of the UUT as required by the TRS.

e. Provides interconnection and switching as required among the UUT, all instrumentation, and power sources.

f. Provides digital communication for control and data handling

between the Line Computer Interface and the station instrumentation and switching circuits.

g. Interfaces the station operator to the computer and the instrumentation and switching circuits.

h. Interfaces maintenance personnel to the computer and instrumentation and switching circuits for diagnostic tasks.

1.2.1.2 Functional Description. The test system is depicted in figure 1-2-1 and the functions of the blocks are described below:

a. The 704 Computer-executes control and UUT programs to accomplish on-line testing or off-line data processing.

b. The Computer Teletype - permits the computer operator to exercise control over program execution during off-line processing or input change directives during on-line testing.

c. The Fixed Head Disc - provides fast access memory expansion during on-line testing for system program and UUT program storage. When used in conjunction with a limited amount of core in a swapping technique it expands the virtual core size to over 400,000 words. It is not available during off-line processing.

d. The Cartridge Disc - provides UUT program storage during on-line testing. It is a Real Time Operating System (RTOS) storage device for all off-line processing.

e. The Line Printer - outputs hard copy documentation during off-line processing. It is not available during on-line testing.

f. The Card Reader - provides a general input medium for reading IBM type 80 column punched cards during off-line processing. It is also available during on-line testing to input UUT programs in object form either for immediate use in the test of a UUT, or for update of the Cartridge Disc UUT program files.

g. The Card Punch - outputs IBM type 80 column punched cards during off-line processing. It is used during program compilation to output UUT programs in object form. It is not available during on-line testing.

h. The Magnetic Tape Transports - provide a long-term slow access bulk storage capability. They are used during system installation to build the Fixed Head Disc and the Cartridge Discs. They are used during on-line testing to collect bulk data from UUT testing and as a storage medium for diagnostic core dumps. They are used during off-line processing to input data which was collected during on-line testing.

i. The Teleprinter Multiplexer and Teleprinters - provide communication channels to the test station operators during on-line testing to output information to the operators and receive directives from the operators. These channels are independent of the LCI-TSI test station data communication channels.

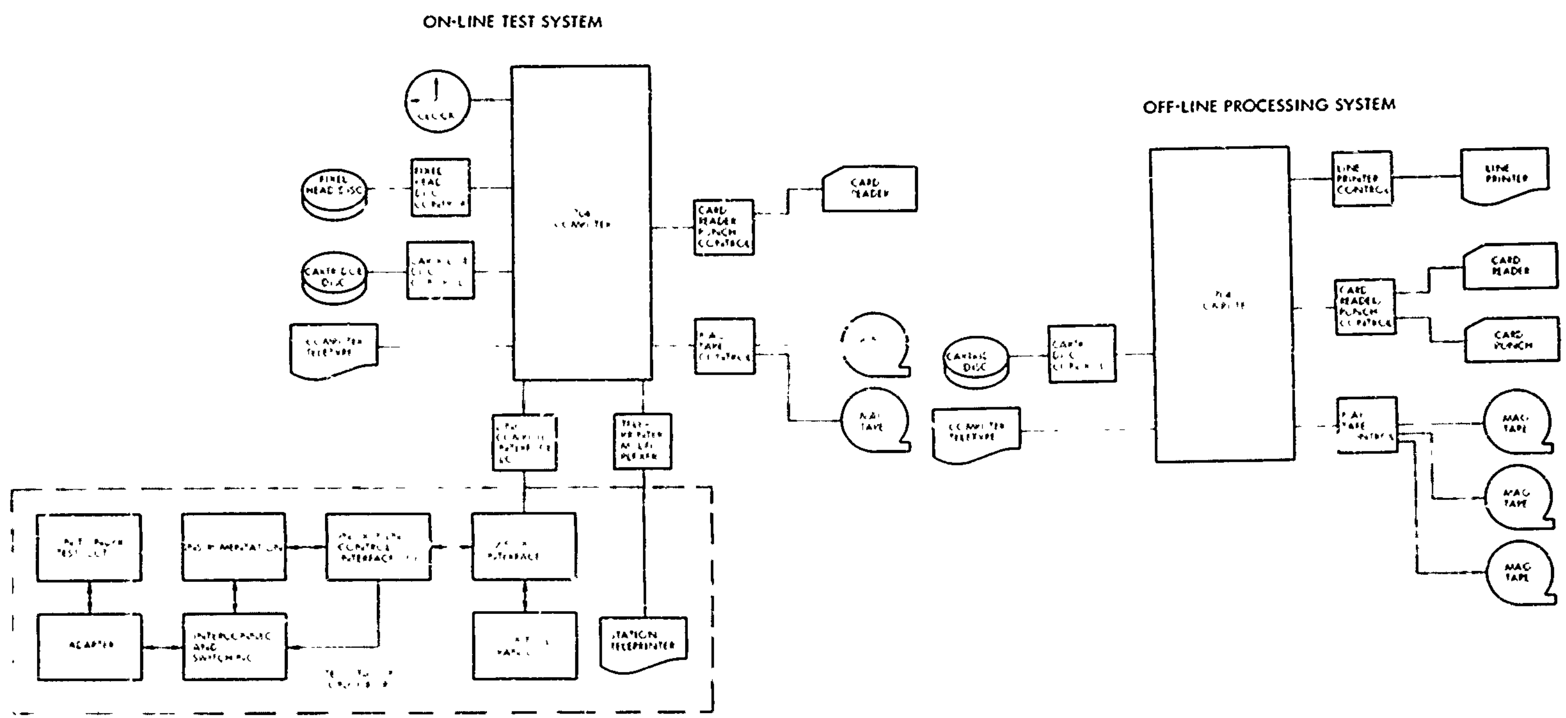


Figure 1-2-1. Improved HAWK Factory Test S·ˢᵗ·ₘ Block Diagram

1-2-5/1-2-6

j. The Clock - provides real time information to the computer for time interval calculations and time of day. It is not available during off-line processing.

k. The Line Computer Interface (LCI) - provides bidirectional data communications between the Computer and the Test Station Interface (TSI). The LCI provides an interface channel for transmitting programming information to the test station and receiving status, interrupt, and measurement data from the test station.

l. The Test Station Interface (TSI) - provides a bidirectional communication interface between the LCI and the test station. It provides and accepts bit-serial data streams to and from the LCI and provides and accepts parallel bit patterns to and from the Instrument Control Interfaces (ICI) and the control panel. The TSI performs ICI selection, interrupt handling, serial to parallel and reverse conversion, timing control, and error checking for each station.

m. The Control Panel - receives test station operator inputs via switches and push buttons and transmits this information to the computer via the TSI - LCI link. It also receives program status from the computer via the LCI - TSI link and outputs the status to the operator via visual displays.

n. The Instrument Control Interfaces - provide level conversion, data storage, format conversion, timing, and control for each programmable device in the test station. It makes each unique device compatible with the standard TSI.

o. The Interconnection and Switching Networks - provide fixed signal and power routing within the station as well as variable interconnections under program control as required among instruments, power sources, and the UUT.

p. The Instrumentation - provides stimuli, power, and measuring capability as required by the TRS.

q. The Adapter - accomodates any unique interface and connection requirements between the test station instrumentation and interconnection system and the UUT.

1.2.1.3 Hardware Description. The principal characteristics of the hardware blocks (refer to figure 1-2-1) which make up the system are as follows:

a. The 704 Computer - has the following features:

32K of 1.0 microsecond core memory
16 bit word with parity
Hardware multiply and divide
16 levels of interrupt
Direct Memory Access (DMA)

b. The Computer Teletype - is an ASR35 TELETYPE with keyboard, ink ribbon type mechanism printing on teletype paper at a 10 character per second rate with 72 characters per line, 10 characters per second 8-channel paper tape reader, and 10 characters per second 8-channel paper tape punch.

c. The Fixed Head Disc. - is a 384,00) word disc with 370,000 bits per second transfer rate and 33 millisecond maximum access time.

d. The Cartridge Disc - is a 1,280,000 word interchangeable disc cartridge with a maximum access time of 180 milliseconds and a transfer rate of 781,000 bits per second.

e. The Line Printer - provides a 132 character per line printout at a 1000 lines per minute rate on up to 6 part fan-fold computer paper.

f. The Card Punch - produces from 100 to 400 IBM type 80 column punched cards per minute.

g. The Card Reader - reads up to 1000 IBM type 80 column punched cards per minute.

h. The Magnetic Tape Transports - provide IBM compatible 75 inch per second tape handling at 800 bits per inch on 3/4 inch computer grade magnetic tape.

i. The Teleprinter Multiplexer and Teleprinters - provide up to 16 remote teleprinter terminals operating in ASCII format. Printout is on rolls of 8 1/2 inch wide thermal paper at 30 characters per second and 72 characters per line. Input is via a standard keyboard.

j. The Instrument Control Interfaces - accept 32 bit parallel data words from the TSI and output the required control signals to the instrument for which they were designed. They receive data from the instruments and forward it to the TSI in 32 bit parallel data words. They also provide timing and control unique to each instrument.

k. The Interconnection and Switching Networks - consist of cables, switching networks, and connectors as required to handle power and signal routing in the test station.

l. The Instrumentation - is commercial stimuli and measuring instrumentation chassis, specially designed stimuli and measuring instrumentation chassis, and control chassis as required by the functions to be performed by the specific test station.

m. The Adapters - are boxes (or platters for IH200) which contain circuits, loads, and interconnections for adapting the UUT to the test station. Any special requirements imposed by the TRS are handled by these devices.

n. The Line Computer Interface (LCI) - accepts data from a queue in the computer in 16 bit parallel computer DIO transfers at the maximum computer I/O speed. It then transmits this data in a bit-serial echo-checked fashion at an 80,000 bits per second rate to any remote test station within 2000 feet. In a reciprocal manner the test station can communicate with the LCI at an 80,000 bits per second echo-checked data rate and the LCI will transfer the received and stored transmission to the computer at its maximum DIO rate under computer interrupt control. The LCI also provides station interrupt information for transfer to the computer under computer interrupt control.

o. The Test Station Interface (TSI) - is the test station end of the data communication channel between the computer and the station. It receives serial data from the LCI and converts it to 32 bit parallel data words which it directs to a selected Instrument Control Interface (ICI) or Computer Control Panel. It receives 32 bit data words from a selected ICI or Control Panel and transmits this data in bit-serial form to the LCI. It also handles operator or instrument interrupts which it passes to the LCI during polling sequences.

p. The Control Panel - is a display an/input panel in the test station having lever switches for inputting part and serial numbers, pushbuttons for inputting status and directives, and lights and numeric displays for outputting program status.

1.2.1.4 Packaging. The Test System is packaged as follows:

a. The 704 Computer is functionally partitioned into modules which plug into an interconnecting backplane. The display and control panel swings out from the front of the cabinet to permit easy access to these modules for replacement purposes. The computer is housed in a standard 19 inch relay rack type cabinet which is in one bay of the computer console. The WANGCO Magnetic Tape Transports and Controller, the Card Reader/Punch controller, the Fixed Head Disc and Controller, the Cartridge Disc and Controller, and miscellaneous power supplies are also mounted in relay rack type cabinets which are part of the computer console.

b. The Clock, Line Printer Controller and Teleprinter Multiplexer are mounted in a peripheral control chassis which is in a relay rack type cabinet as part of the computer console. This peripheral control chassis contains a wire wrapped backplane into which the functional modules are plugged. The functional modules are wire wrapped circuit cards holding up to 60 standard dual in-line packaged (DIP) Intergrated Circuits (IC's). These circuit cards are the same design as those used to package the TSI and ICI's in each test station. They are easily replaceable for low system MTTR (Mean Time To Repair) yet are easily repaired due to plug-in IC's. One or more functional modules are required to implement each major sub-system.

c. The Line Computer Interface (LCI) is packaged in a 19 inch relay rack type cabinet in the computer console. This sub-system is packaged on wire wrapped backplanes having plug-in IC sockets to accomodate a large number of DIP IC's. There is one large backplane and two foldout smaller backplanes to complete the chassis. The IC's are upside down in operation with the backside wiring of the backplane exposed for ease in troubleshooting and signal tracing.

d. The TSI is packaged in a logic basket in the back of each test station. It is distributed over two wire wrapped circuit cards each of which can hold up to 60 IC's. Each of these cards contains a 120 pin I/O edge-of-card connector for backplane interface and an 80 pin edge-of-card connector for cable interface. The ICI's are packaged in similar fashion such that the logic basket is tailored to a specific station configuration merely by plugging in the appropriate modular ICI's. All other aspects of the logic basket are standard and do not change from station to station.

e. The Line Printer is a specific cabinet aas is the Card Punch and the Computer Teletype. These are free standing units attached to the computer console by cables.

f. The Card Reader is a table top unit which connects to the computer console with a cable. The test station teleprinter is also a table top unit connected to the test station via a cable.

g. The Control Panel is a 19 inch relay rack type chassis that is installed in the test station in a location convenient to the operator.

h. The instrumentation is generally packaged in 19 inch relay rack type chassis as built by the vendor. These chassis are located, with due regard to function, within the bays of the station console.

i. The interconnection cables and switching networks are packaged in varying forms as the test station needs require.

j. The computer console, line printer, card punch, card reader and Computer TELETYPE are located in an air conditioned area of approximately 70 square feet. Each test station and its associated table top teleprinter can be remotely located up to 2000 feet from this computer complex. The stations are connected via three 95 ohm twisted shielded twin conductor cables. The teleprinters are connected via three wire telephone cables.

1.2.2 Software Structure

1.2.2.1 Test Operating System - General. The Test Operating System was developed to respond to the many design objectives of a quasi real-time operating system functioning as the central control media of an overall test system. The software modules function in this capacity via a series of planned interactions which achieve the end result - run the test stations by executing a UUT program and thus test parts. The dissertation which follows attempts to show these interactions and to establish for the reader a philosophical background in the software operation. Some poetic license is taken to avoid the depth of detail which would tend to cloud the overall understanding.

One of the prime considerations in the development of the test operating system was the division of tasks between the operating system and the UUT program. The more functions adopted by the system, the less repetitive tasks had to be performed by the UUT program. When tempered by the constraints of a mini-computer with its relatively limited computation and memory capability, a system of common execution packages evolved. All of the blocks shown in Figure 1-2-2 (unless otherwise noted) are in core at all times (resident operating system). Both the control and execution sections are utilized by each UUT program as it executes in turn. The disk is used by the system to bring UUT programs and selected portions of the operating system in and out of core - but more on that later.

1.2.2.2 Functional Organization & Description. The Test Operating System consists of a series of core resident routines designed to control the dynamic scheduling of events within the computer and provides the interface between the Unit Under Test (UUT) program and the computer peripheral and/or test station hardware. These functions are accomplished through the following specific routines. (Reference Figure 1-2-2).

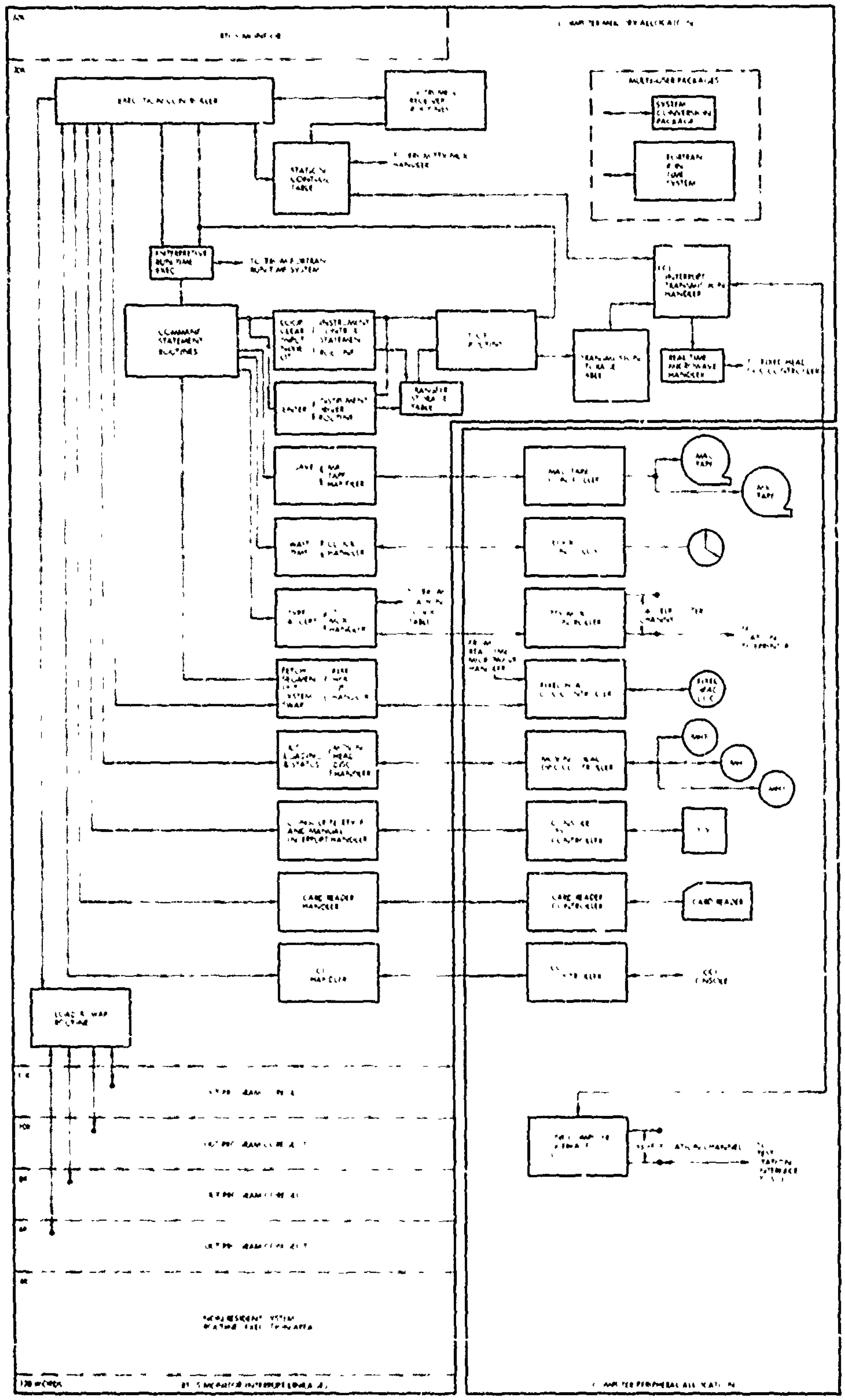


Figure 1-2-2. Computer Test System, Block Diagram (Sheet 1 of 2)

1-2-13/1-2-14

a. Execution Controller - The Execution Controller controls the sequence of execution for all programs and routines by continually scanning a table of information (Test Station Control Table) pertinent to the status of each test station and the UUT program being utilized by that Test Station.

b. Interpretive Run Time Executive - The Interpretive Run Time Executive Routine interprets the output of the TECOM Compiler and transfers control to the designated routine, either the Fortran Run Time System Package or to the Command Statement Routines.

c. Command Statement Routines - The Command Statement Routines a.. the execution packages for the test oriented TECOM Compiler statements (i.e., ENTER, MEASURE, LOOP, etc.). They transfer control to the designated Instrument Driver or Peripheral Handler.

d. Instrument Drivers - The Instrument Drivers control the generation of data to be transmitted to a given instrument and passes it to the Test Station Output Transfer Routine through the Transfer Storage Table (XFR1).

e. Test Station Output Transfer Routine (TSOT) - The TSOT Station Output Transfer Routine appends routing information to the transmission stored in the XFR1 table. The final transmission is queued in the Transmission Storage Table (TST) for transmission by the Line Computer Interface Handler.

f. Line Computer Interface Handler - The Line Computer Interface Handler controls the flow of transmissions from the Transmission Storage Tables to the Test Station via the Line Computer Interface (LCI); and controls the retrieval of data from the Test Station instruments and stores it in the Test Station Control Table.

g. Instrument Receivers - The Instrument Receiver Routines control the conversion of the data returned from the instruments through the Test Station Control Table.

h. Peripheral Handlers - The Peripheral Handlers, Magnetic Tape, Clock, Teleprinter Multiplexer, Fixed Head Disc, Moving Head Disc, Console Teletype, and Card Reader, control the data transfer between their respective devices and the core memory.

i. Computer to Computer Interface Handler - The Computer to Computer Interface Handler controls the data transfer to and from the other computers when the system is structured in a multi-computer configuration.

j. Real Time Microwave Handler - The Real Time Mircowave Handler controls the transfer of data directly from the LCI Handler to the Fixed Head Disc Controller.

k. Load and Swap Routine - The Load and Swap Routine controls all core and Fixed Head Disc allocation requests made by the execution controller. The Load and Swap Routine enables the Operating System to function as if it had unlimited core memory (over 400,000 words of virtual memory).

l. Unit Under Test (UUT) Programs - The UUT Programs are interpretive level programs written in the TECOM language which consist of a

sequence of control instructions to be executed by an automatic test station to determine the acceptability of a UUT.

m. Non-Resident Systems Routines - The Non-Resident System Routines are subroutines used only by the execution controller. They are written as re-entrant, self contained packages which are loaded into core as needed.

n. Multi-User Packages - The Multi-User Packages are utility subroutines used by many of the operating system routines; as a result, the many interconnections are not shown in Figure 1-2-2.

1.2.2.3 <u>Fixed Head Disc Storage Organization and Description</u>. The Fixed Head Disc is the principal input device for the loading of the Test Operating System. The disc is divided into three distinct sections as shown in Figure 1-2-3.

The first section contains all needed processors to perform the loading of the Test System (i.e., RTOS, XRAY, QUEUE, and LOADER). These processors are under the control of the Real Time Executive (XRAY) and use the Real Time Operating System Monitor (RTOS). This section also contains the diagnostic packages used to maintain both the central processor and all associated peripherals.

The second section contains all routines, packages, handlers, etc., which comprise the Test Operating System. They are written and stored in relocatable text. The Test Operating System (packages, handlers, routines, etc.) is loaded into core by the relocatable loader (RESLOAD) via the XRAY directives:

- o Resident Subroutines (RS)
- o Resident Task (RT)
- o Queue, Load and Execute (QU)

The third section of the disc (all remaining sectors) is subdivided into four logical files as part of the Test Operating System initialization. File zero is again subdivided into two subfiles used as temporary storage by the UUT load routine, and as temporary storage of UUT programs by the UUT swap routine. File one is used to store (in ABSO form) the Non-Resident System Routines loaded during system initialization. File two and three are used as temporary storage of Real Time data by the Real Time Microwave Handler.

1.2.2.4 <u>Moving Head Disk Organization and Description</u>. The purpose of this section is to describe the configuration, content, file structure and access technique for the moving head disk, Figure 1-2-4.

The moving head disk may vary in unique installation configurations but must have a minimum of one (1) and may have a maximum of four (4). Each disk is addressed as a unique unit by Moving Head Disk Handlers.

The content of the disk(s) is arranged into three (3) major categories:

a. Off-line Processing Bootstrap and System
b. Indexed Sequential File Descriptor and Key Indexes
c. uUUT Program Object Text

The Off-line Processing Bootstrap and System resides on disk zero (0) in approximately the first two hundred (200) sectors. It contains the off-line

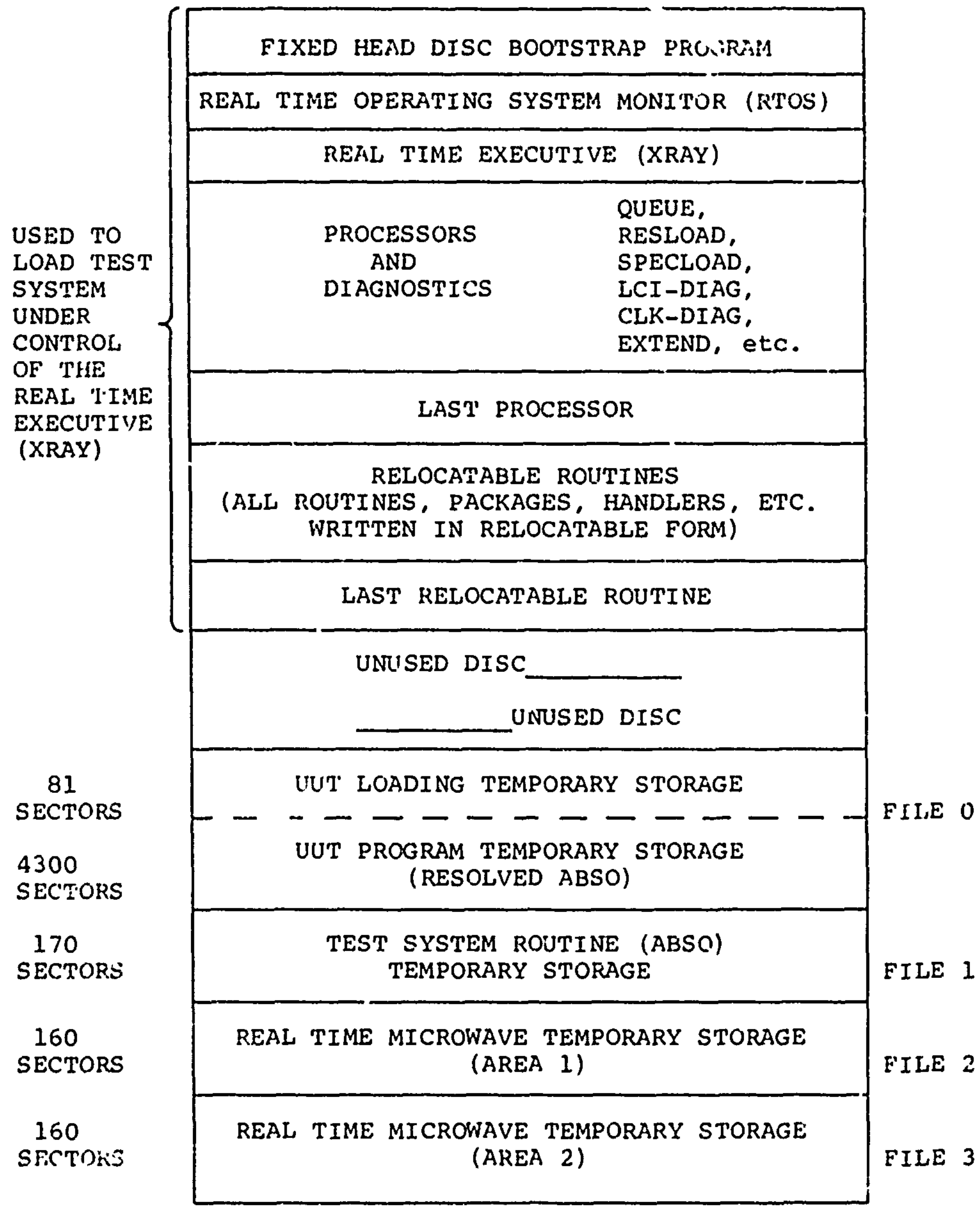


Figure 1-2-3. Fixed Head Disc Storage Organization

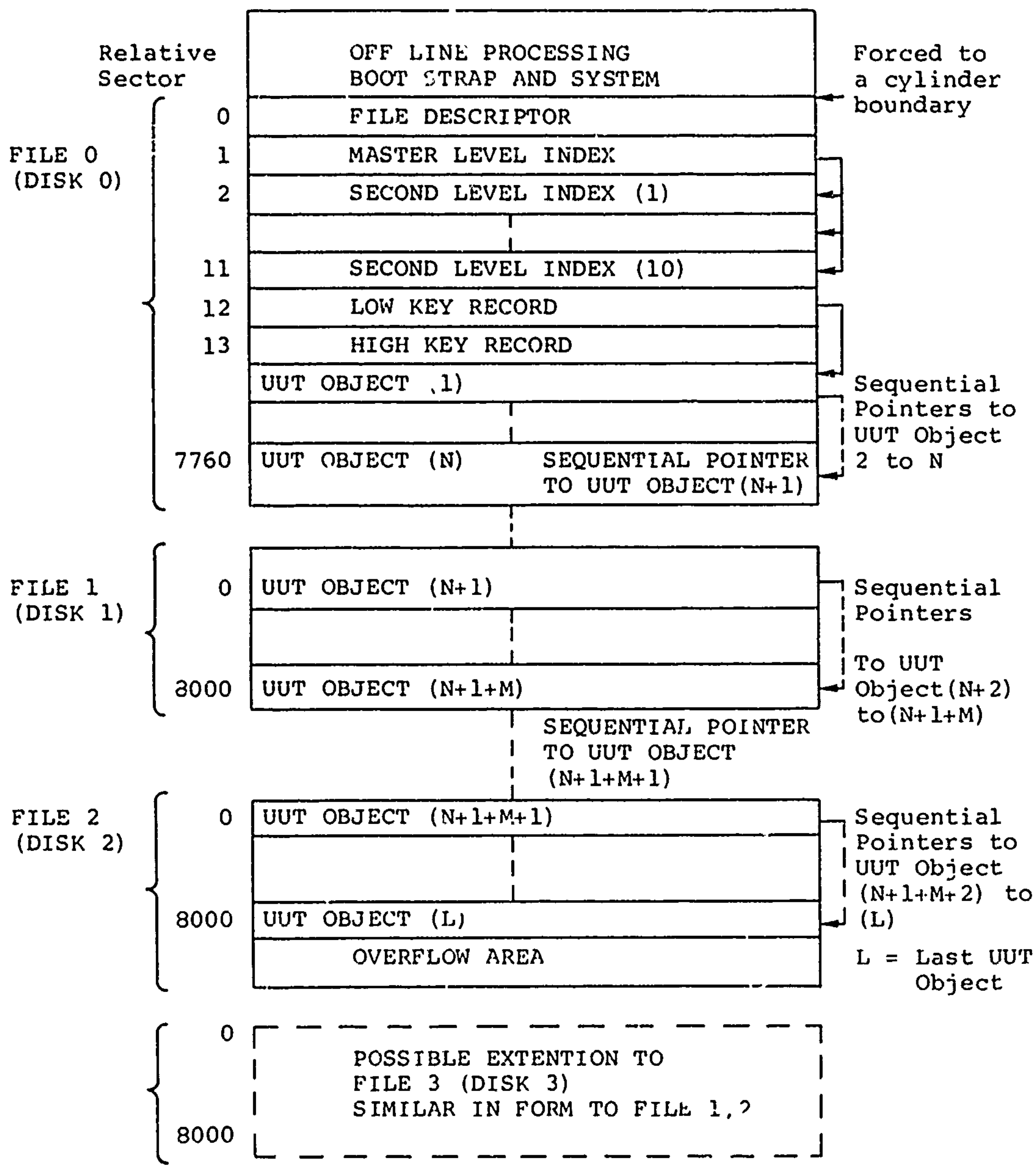


Figure 1-2-4. Moving Head Disk File Structure
(Indexed Sequential)

moving head disk file operating system (DFOS), and processor packages (XRAY, QUEUE, and DSKDMP) to support the off-line function of printing a requested sector or sectors of the multi-disk file on the Line Printer.

In as much as the major body of the moving head disk(s) is arranged in sequential file organization, an area is appropriated to file description and key indexes. The file descriptor is a one (1) sector area located on the cylinder following the OFFLINE Processing Bootstrap and System and contains information regarding size(s) of file(s), number of entries in the file(s) and sector pointers required by the disk handler routine. The sector which follows is allocated to a primary (master) index of part number keys and their respective sector pointers to secondary (second level) key indicies in which the actual UUT Object Text will be found. There is one master index key-pointer set for each second level sector. The next ten (10) sectors are reserved for key-pointer sets (second level) that point to specific sectors of the file(s) wherein the UUT Object Text resides. The actual UUT Object Text in Header-Text format occupies the remainder of the fields).

The entire file, from one (1) to four (4) moving head disks, is treated as a single continuous file with relation to the key-pointer indexes and is arranged in part number sequence for access.

The access of information from the Moving Head Disk Controller is via the Moving Head Disk Handler routine which upon receipt of a request for a specific UUT object program performs the following functions:

For each request the file descriptor is examined for information regarding file size, location of indexes and other pertinent data required for search. The primary index (master) is read next and scanned to find the sector address of the proper secondary (second level) index. The identified secondary index is read and scanned to find the sector address at which the UUT Object Text Header is located. Finally the header and appropriate object text is read for transmittal to the requester.

4.1 TEST DATA RETENTION

4.1.1 Data Logging

The IH Test System automatically logs test data on magnetic tape as part of the test execution. The Test Operator is provided control over test data retention via a "Save No Data" switch which is integral to the control panel. Illumination of this switch causes the system to restrict its retention to a header record (used to identify test station activity when the station is being used and for what purpose it is being used). The operator is notified via the teleprinter that test data is not being retained. This is done to prevent accidental testing without data retention. The "SAVE NO DATA" switch only has control over logging (parametric data is still compared to specification and accept/reject decisions are still made even when the switch is illuminated). In its normal state the switch is not illuminated. All parametric data is stored at the point it is compared by the UUT program and the test system subsequently logs the data onto magnetic tape. Test data is always available on the Teleprinter at the operator's discretion.

4.1.2 Test Data Buffer Construction.

The logging process employed by the test system involves constructing a test data buffer which is appended to the UUT program. The header portion of the buffer is built-up as each test is initiated. Assuming the "Save No

Data" switch is not illuminated, additional information is posted by the test system when an "INIT" statement is encountered and test data reading increments are appended as each "Save" data statement is encountered in the UUT program. The process continues until the buffer is filled at which time the buffer is logged to tape. When the program is terminated, accept/reject disposition and stop test time are posted to the header.

4.1.3 Data Transfer

The actual transfer of data to magnetic tape is a function of the computer configuration being utilized. In a single computer configuration, the test data buffer is logged directly onto the tape. In a multi-computer configuration with line and collection computers. the data is transferred from the line computer(s) to the collection computer via the CCI. The data is read into special buffer storage areas provided for this purpose and is transferred to tape.

Since data buffers fill asynchronously, the actual sequence in which test data records are logged onto tape, is random. Off-line processing is required to resequence the data tape into a format which can be processed in the classical fashion. Reporting and analysis programs also are available for producing management and engineering reports.

5.1 TECOM (Test Compiler) is a procedure oriented language for generating programs to perform acceptance and/or alignment tests on assemblies or subsystems typical of a sophisticiated weapons system. The programs direct an automatic test equipment system containing a configuration of programmable instrumentation which apply stimuli and obtain measurements from the unit under test (UUT). The programming process consists of translating the procedures for testing UUT's into TECOM Programs which automatically or semi-automatically conduct the unit tests.

The TECOM language is comprised of two groups of statements. The statements of one group resemble several FORTRAN statements (e.g., DIMENSION, DO, arithmetic IF, etc.). This group provides common engineering expression. notation, and program control capabilities required to solve the test problem.

Special function statements comprise the second group. These allow the engineer to select such functions as:

- o Address required instruments and define their function, range, etc.
- o Route stimuli and measurement instruments to the UUT.
- o Specify numerical limits and tolerances.
- o Generate the commands which start, measure and control the test.

The major benefit of TECOM is that the engineer can program his test requirements in a language which appears natural for him using only common engineering vocabulary terms. In addition, the engineer is relieved of the responsibility for repetitive control functions (i.e., program start up, data limit specification, data retention, pass-fail decisions, etc.) by making these system tasks controlled by the UUT Program. The higher level language aspect of TECOM minimizes engineering training time, reduces programming and debugging time, and also makes the test program self documenting.

REFERENCES

1. Extracts from the "Improved HAWK Factory Test Computer System" manual Raytheon Company Missile Systems Division, Andover, Massachusetts.

APPENDIX B

A Distributive Intelligence Factory Test System for Electronic Assemblies

INTRODUCTION

Sophistication of modern electronic equipment and the stringent reliability standards imposed by the military have resulted in the development of a Distributive Intelligence Factory Test System used in the manufacturing process of electronic assemblies for the SAM-D missile system. SAM-D is a US Army Missile system with major new capabilities that has as its mission air defense of the field army in the 1980-and-beyond time frame (1,.2). Assemblies tested range in variety and size from microcircuits to phased array radar antennas.

A major design feature of the test system includes the utilization of modularized hardware and software construction techniques to facilitate maintenance, system expansion, and system flexibility (3). A standardization program for commonality of instrumentation, program language, mechanical configuration, and test adapters minimizes station design effort, simplifies the software generation, and enhances the maintainability and maintenance logistics of the entire test complex. These philosophies are based on the experience gained in another successful test equipment system designed for factory testing of electronic assemblies - the Improved Hawk Automatic Test System (4).

This paper presents the system overview and a general description covering the characteristics and responsibilities of each major functional area. Subjects include the test system organization and operation, test data processing, the RATEL programming language in which UUT (unit under test) programs are written, UUT program characteristics, and station support software.

SYSTEM OVERVIEW

The factory test complex is configured as a two-level hierarchy of computer systems (Figure 1). At the top level, a Central Computer system performs supervisory control activities over the second level - a network of remote Automatic Test Centers or Stations that perform the test requirements.

The Central System, operating on a time sharing basis, is responsible for not only maintaining a complete library of UUT programs and support software packages for distribution to the test centers but also for formatting and recording of test data sent from the test centers.

The Test Centers are structured as "Intelligent Terminals" with their own Process Controllers for providing real-time local control of UUT test sequences. The major responsibility of the Test Centers is to perform UUT testing. This involves executing a test sequence, evaluating the response from the instrumentation, determining the responses' acceptability, and

requesting transfer of the test results to the Central System for permanent storage. Other responsibilities include debugging all on-line station/UUT hardware, compiling and editing source text requested from the central system, and coordinating all communications between the Process Controller and the Central System.

Stations are configured for testing electronic assemblies that have compatible characteristics (e.g., analog, digital, etc.). Consequently, while sharing many common design features (particularly communications and software), the Test Centers differ in the specialized instrumentation necessary to perform the particualar test function (i.e., analog instrumentatio for analog assemblies).

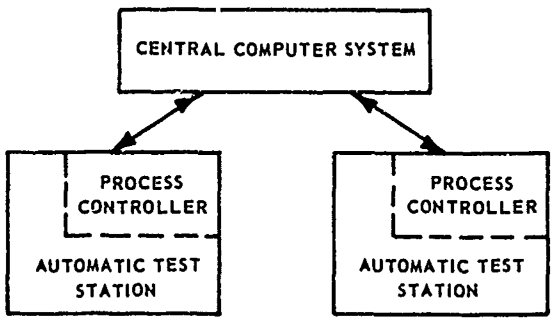


Figure 1. Factory Test System

CENTRAL SYSTEM ORGANIZATION

The major hardware components comprising the Central System as shown in Figure 2, include a Raytheon 704 computer with 32K 16 bit words of core memory, a custom designed Multiplexer communication link to all the Automatic Test Stations, an Information Storage System model 714D disk with 13 million words of storage, two 9-track Pertec magnetic tape units, an 80 column 300 lines/minute Data Products line printer, a Documation model 1000 card reader, an ASR35 teletypewriter, a special design digital clock, and a Calcomp model 565 digital plotter.

The Central Computer controls the storage and retrieval of UUT programs performs data collection, and provides managerial control over the entire test complex. The Multiplexer provides the communication link between the Central Computer and the network of Process Controllers at the Test Centers. The Disk provides permanent storage for UUT programs as well as the test station support software (compiler, editor, etc.). The Tape units are used to log all system activities and test results from the test centers for later off-line processing. The Line Printer produces the hard copy listings for test data and UUT programs. The Card Reader serves as the primary input device for entering on disk new UUT programs and special data bases. The Teletype provides an interactive man/machine interface link to the Central System operations. The Digital Clock is used by the Central System during activity logging and is accessed by the test system for monitoring

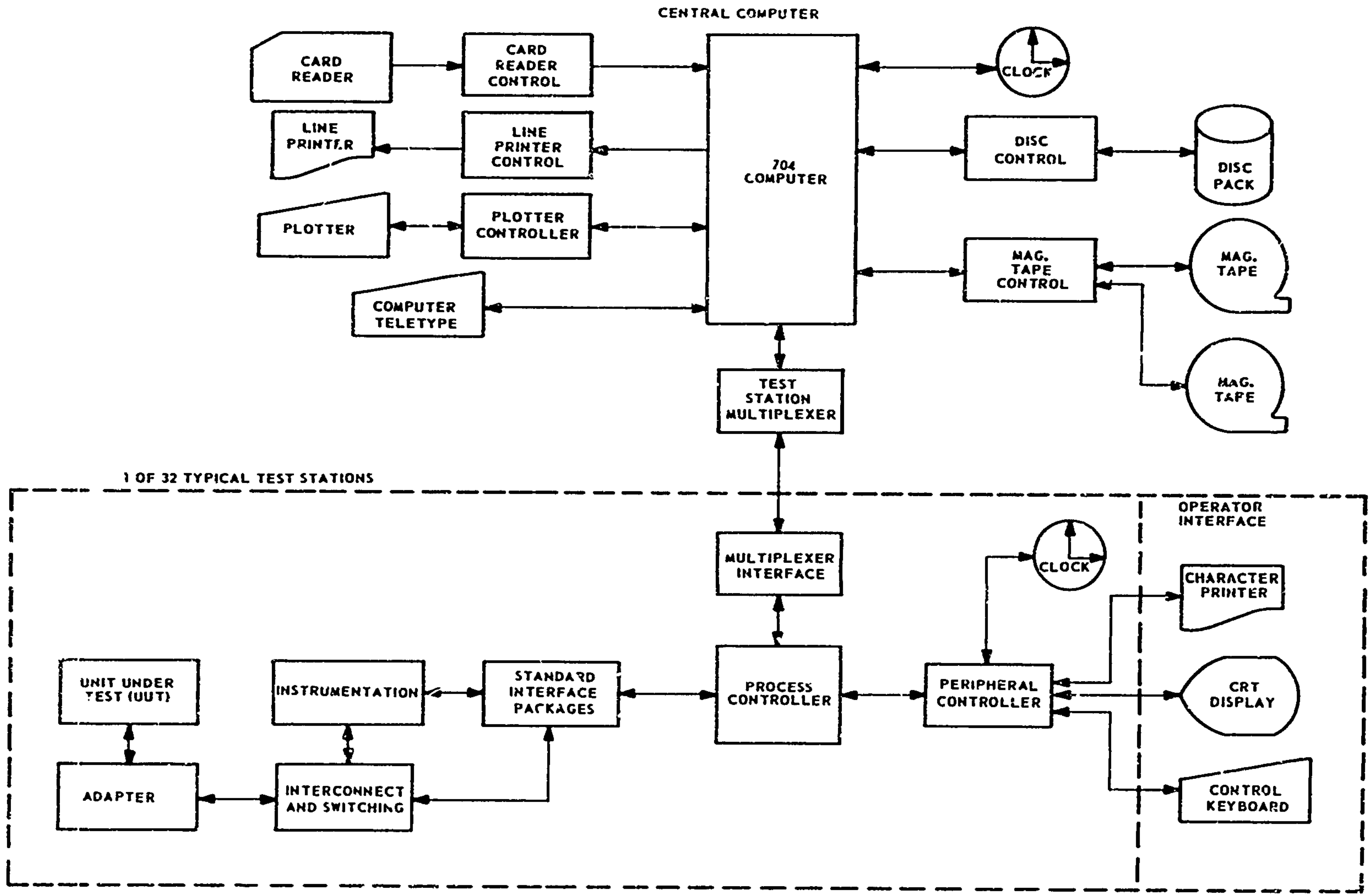
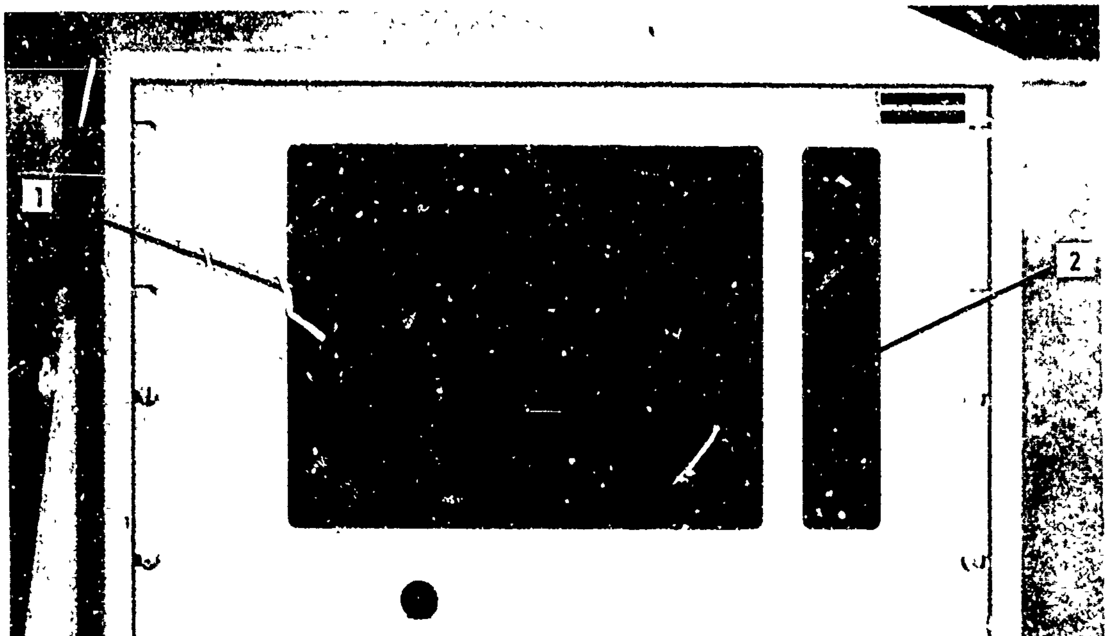


Figure 2 SAM-D FACTORY TEST SYSTEM BLOCK DIAGRAM

FIGURE 3. HIGH FREQUENCY ANALOG TEST STATION



1. DATA SCREEN
2. SPECIAL FUNCTION DISPLAYS
3. PRINTER
4. ALPHA NUMERIC KEYBOARD
5. CURSOR CONTROLS
6. OPERATOR SPECIAL FUNCTION KEYS

FIGURE 4. OPERATOR INTERFACE TERMINAL

of time dependent events. Hard copy graphic plots of UUT test data and other pertinent information can be obtained via the Digital Plotter.

TEST CENTER ORGANIZATION

The major hardware components comprising a typical test center also shown in Figure 2, include the Process Controller - a Raytheon 704 computer with 28K 16 bit words of core memory, a custom designed Multiplexer Interface, a custom designed Standardized Interface Package (SIP), and an Operator Interface Terminal (OIT) consisting of a TEC model 415 message oriented Data Screen with an alphanumeric keyboard and full cursor control, a set of Operator Special Function Keys, an Operator Special Function Display Panel, and an 80 column 30 character/sec TI model 722S Printer. In addition, each Automatic Test Station contains the necessary set of commercially available programmable and non-programmable stimulus/measurement instruments required to support the desired testing function. A programmable switching matrix unit interconnects the station instrumentation to the UUT via a UUT adapter unit that is interchangeable and programmable. Figure 3 shows one of the Test Centers and figure 4 shows a closeup of an OIT. Figure 5 details the Operator Special Fumnction Keys and Cursor Controls.

CURSOR CONTROLS & 2 FUNCTION KEYS

DSL	CS	CM
IC	↑	IL
←	HOME	→
DC	↓	DL
LOOP	EEOL	EEOP

FUNCTION KEYS

STOP	ATTEN	SEMI AUTO	ABORT
STEP	MEAS	TEST	REJ DATA
PAUSE •	DISP	PRINT	ALL DATA
YES	NO	CONT	REPEAT

Fig.5 Cursor Controls & Operator Function Keys

The Process Controller performs all the test control and man/machine interface functions at the test center. The Multiplexer Interface unit completes the communication channel between the Central System and the Process Controller. A hardware bootstrap is provided to initially load the local Process Controller. The SIP hardware provides the control interface between the Process Controller and all programmable instruments. The OIT accomodates the human interface to the test stati processor. The CRT provides for visual directives, the Keyboard for data entry by the operator, the set of Special Function Keys for entry of operator options during testing, and the Special Function Display for status reporting of these options. The Station Printer is used for selective hard copy data reporting as required by the operator.

FACTORY TEST STATION CONFIGURATIONS

Presently, eight station configurations are available for testing the following categories of Electronic Assemblies:

- Digital Modules and Microcircuits
- Pulse/Analog Modules and Microcircuits
- Interconnecting networks (substrates and Printed Wire Boards)
- High Frequency Analog Modules and Microcircuits
- Digital Subsystems
- Missile Uplink Decoder Tray
- Antenna Elements
- Radar Antenna System Group

To fully comprehend the scope of the testing problem, a synopsis of each station follows:

Digital Station - tests high speed (up to 10 MHz) modules and microcircuits performing a) dynamic functional tests (exercise a digital device by applying a predetermined binary pattern at typical operational speeds and observing the logic response). b) DC parametric tests, c) propagation delay tests.

Pulse/Analog Station - tests modules and microcircuits (pin configurations from 14 to 120 pins) which require detailed waveform analysis. The station provides sinewaves, squarewaves, and ramps at frequencies ranging from 1 Hz to 10 MHz and pulse stimuli from 10 Hz to 10 MHz with pulse widths from 10 NS to 10 MS. UUT measurements are made for periods, frequencies, Rise/Fall Times, progagation delays, overshoots/undershoots, DC Resistances, DC/AC voltages, time to voltage levels., time between voltage levels, storage times, AC/DC currents, offsets/amplitudes, and VRMS tests.

Continuity/leakage Station - tests substrate and printed wire boards performing a) Leakage tests (detect up to 1 Megohm shorts), b) Continuity tests (no run exceeds 5 Ohms), and c) Resistance tests (Ranges of 10 Ohms to 10 Megohms).

High Frequency Analog Station (see Figure 3) - tests modules and microcircuits requiring RF response measurements in the frequency range of DC to 500 MHz with RF levels of -114 DBM to +33 DBM and DC voltages of 0 - 50.0 Vdc. UUT measurements include Gain/Insertion Loss, Bandwidth, Phase, I/O VSWR, group delay, dynamic response, noise figure, switching time, frequency/period, intermodulation distortion, DC voltage, and Pulse response.

Digital Subsystem Station - tests a wide variety of assemblies composed of digital modules and microcircuits. The heart of the test station is a custom designed High Speed Interface Controller (HSIC). The HSIC is a 72 bit wide (partitioned into an 8 bit control section and a 64 bit data section), 256 word deep stimuli random access memory and a 72 bit wide, 256 word deep response random access memory. The HSIC can present to the UUT up to 64 lines of information in parallel, or up to 32 bits in serial as well as monitoring up to 64 lines of information from the UUT. The HSIC together with a frequency counter/timer, oscilloscope, power supplies, and pulse generators determine a UUT's response.

Missile Uplink-Decoder Station - is dedicated to testing the uplink-Decoder Missile Tray, this unit performs the switching and control functions of

the missile from pre-launch through the mission. A custom designed Data Generator Panel provides all the necessary inputs to the Uplink-Decoder and together with the station instruments (counter/Timer, DVM, Oscilloscope, Power Supplies) determines the unit's response.

Antenna Element Microwave Station - tests the Phase Shifter Element Assemblies of the SAM-D phased array antenna. The station provides the required RF power (C-Band Sweep Oscillator, Microwave Amplifier, microwave panel to control the RF signal, and frequency counter) to the element assembly. Element measurements include transmission characteristics (both amplitude and phase) as well as reflection characteristics (amplitude and phase). Both single frequency and swept frequency measurements can also be made with the system.

Radar Antenna System Group (RASG) Station - is dedicated to testing all the phased array antennas of the SAM-D Ground Radar Systems. The station a) verifies the response of a Peripheral Electronics Assembly (PEA) box of the radar to simulated status signals, which would reflect most system conditions, b) uses a RASG test set to load data into beam steering storage register modules of the radar and subsequently sending the data back to the test system for verification. c) checks out the PEA performance by monitoring antenna row and column outputs, and finally d) verifies the capability of the PEA box to perform phase shift element built in tests.

AUTOMATIC TEST STATION OPERATION

An Automatic Test Station operates on a "Sign on/Sign off" basis. The operator "Signs On" by selecting a UUT program and one of several modes of operation: Test a production unit, troubleshoot a UUT, or program maintenance (Compile, Edit functions). Each mode configures the station to the selected activity, blocking other activities until the current mode is "Signed Off". A special diagnostic mode is available for exercising and troubleshooting all station hardware.

When production testing, the station communicates the program request to the Central System via the station Multiplexer. The Central System searches the Disk for the correct authorized program and transmits it to the requesting test station. Software interlocks exist between the UUT program, Central System, and the test station such that programs can only be executed on the test station to which they apply. The station then executes the test requirements, makes accept/reject decisions, and transmits test data back to the central facility for analysis and retention. Finally, the operator "Signs Off" his activity, and the station returns to a quiescent state awaiting the next mode selection.

If the UUT being tested requires special manual instrument adjustments or settings, instructions are sent to the operator by the UUT program via the CRT. The operator performs the desired action and program execution resumes.

Two major station features are the "SEMI-AUTO" and "ATTENTION" operator options (two of the special function keys - see Figure 5). Selection of "SEMI-AUTO" allows the operator to alter, via keyboard directives, the current programmed state of an instrument. Selection of "ATTENTION" (mutually exclusive with "SEMI-AUTO") allows the operator to display the last programmed state of any instrument, to display the instrument routing showing the various programmable interconnections of AC/DC signals between

the test system and the UUT, and to trace the execution of a UUT program. Both options serve as useful tools when debugging UUT programs.

The following short list of additional station features provides an insight into the flexibility of the test operating system. Most features are combinations of operator options (refer to Figure 5) which can be exercised concurrently.

- Suspend testing operations (STOP), allowing options to be initiated/terminated, and then resume (CONTINUE)
- Terminate program execution (ABORT)
- Print both accept and reject test data (PRINT + ALL DATA)
- Display both accept and reject test data (DISP + ALL DATA)
- Suspend operations when a failed reading is encountered (PAUSE @ + REJ DATA) and then resume (CONTINUE)
- Execute a single test instrumentation directive (PAUSE @ + STEP) followed by a series of (CONTINUE's)
- Execute a single test sequence of directives (PAUSE @ + TEST) followed by a series of (CONTINUE's)
- Continually execute a series of test directives (execute up to end of loop and set its position (LOOP), then begin program again executing single step up to the start of the loop and set its position (DSL).
- A UUT program can request the operator to respond to a test statement (YES or NO).
- A UUT program can request the operator to respond to a test statement (REPEAT or CONTINUE)

TEST DATA

One of the most significant benefits of an automatic factory test system lies in the common recording, retention, and analysis which can be applied to the test data. As the data is received from the station instrumentation, it is validated (value is compared to applicable specifications) and converted into standard engineering units. The data is then sent to the Central System along with identifying information (units of measure, test number, test reading, accept/reject decision) for temporary storage on Disk. At the completion of a UUT test, a Pass/Fail indication is applied to the test data, and then the entire data record is transferred to tape. A list of serial numbers and their Pass/Fail indications is maintained in the Central System for the "lot" being tested. At the completion of the "lot", a list of UUT serial numbers along with their Pass/fail statistics are furnished to production control personnel.

At regular intervals, the test data tape is put through off-line processing for adding the collected test data to the historical file and for producing daily and weekly test activity management reports. Analysis programs are also available to report on selected data of interest.

THE RATEL PROGRAMMING LANGUAGE

UUT programs are written in a Raytheon Automatic Test Equipment Language called "RATEL". RATEL is a FORTRAN based Interpretive Language designed for both analog and digital test problems. It includes nearly all the capabilities of Raytheon 704 FORTRAN IV and SYM II (Assembly Language).

RATEL provides to the user two related language processors. The first is a one pass Compiler that translates the RATEL version of the program into an interpretive language version of the program. The second processor is a Run Time System Interpreter which executes the interpretive language program generated by the Compiler. A unigue aspect of the RATEL Compiler is its ability to perform full Syntax editing-minimizing the possibility of generating code which might place a test station in an unstable state.

Five basic groups of Data Structures are defined:

- Single Precision Integers
  - -16 bit decimal (-32768 to +32767)
  - -16 bit hex (X'0000' to X'FFFF')
  - -15 bit octal (Ø'00000' to Ø'77777')
- Mid-precision floating point reals (-10**38 to +10**38)
- Alphanumerics (up to 12 characters)
- Bit patterns (up to 96 bits) generated in terms of
  - -Hex (4 bits/digit-max 24 digits)
  - -Octal (3 bits/digit-max 32 digits)
  - -Binary (1 bit/digit-max 96 digits)
- Binary fields (up to 96 bits) generated in terms of "0's", "1's" and "X's" (Don't Cares)

RATEL supports complete alphanumeric manipulation. A special data type, ALPHA, allows the programmer to directly manipulate alphanumeric strings. Special statements replace one string or substring with another, convert an integer value into its alphanumeric equivalent, and compare two strings branching on the result.

RATEL also supports complete bit pattern operations. A special data type, BUFFER, allows the programmer to directly manipulate bit patterns. The bit operations are performed either on a single parameter (shift left/right logical, shift left/right circular, invert, 2's complement, and an end-end reversal) or between two parameters (add, substract, multiply, divide, logical and, exclusive or, and inclusive or). A special statement, LET, is used in place of the normal assignment statement for replacement operation. A unique feature of RATEL is the ability to reference selected bits within a bit field. A special data type, REGISTER, allows the programmer to directly access and operate on any bit groupings (in any order) as though the entire group were a continuous block of bits.

Another feature of RATEL is that of program segmentation. When a UUT program becomes too large to incorporate in a single program load, the programmer can divide it into smaller independent sub-program units called "SEGMENTS" (maximum of fifteen). The complete program is executed one segment at a time, called in any desired order (not necessarily Seg 1, ... Seg. 15) or frequency. A fundamental concept to segmentation is that of Global and Local variables. Global variables are those defined in the main program of the first segment and are accessable from any part of the program (other main programs, subprograms and segments). Local variables, however, are those defined within subprograms and segments (other than the first) and are accessable only to the subprogram unit in which they are defined.

The test capabilities are provided by an extensive selection of test oriented verb type statements divided into seven categories (see Table I). The following paragraphs outline the RATEL test statement highlights.

Instrument Control Statements - direct the actions of programmable instruments. They include the following operations:

I. Instrument Control Statements

Clear	-	Reset an instrument or station
Enter	-	Set up an instrument
Loop	-	Pur an instrument in a local loop mode
Input	-	Take Data from an instrument

II. Matrix and GPR Communication Statements

Latch	-	Close a Matrix point
Unlatch	-	Open a Matrix point
DEFMXT	-	Define an association between Matrix points(s) and alphanumeric symbol(s)
SETGPR	-	Set "1" to the indicated GPR bit position(s)
RESGPR	-	Set "0" to the indicated GPR bit position(s)
DEFGPR	-	Define an association between GPR bit position(s) and alphanumeric symbol(s)

III. Time Control Statements

DELAY	-	Wait a period of time
TIME	-	Get Time of Day

IV. Program Control Statements

TERM	-	Normal completion of test
ABORT	-	Signify abnormal completion of test
REPCO	-	Ask operator for a REPEAT/CONTINUE decision
YESNO	-	Ask operator for a response YES or NO
SENSE	-	Sense a software/hardware switch
SEGMNT	-	Retrieve a program segment
TEST	-	Define a test number, name, and reading count
SANDS	-	Spec and Save numeric data
SBD	-	Retrieve a classified frequency
GETAD	-	Retrieve adapter code

V. Table Processing

CATDB	-	Catalogue a data block
GETDB	-	Retrieve a data block

VI. Non-Direct Read-out of Instruments

MEAACV	-	Measure the ACVM Ballantine 3571
MEASWG	-	Measure network analyzer - GR1710
MEAVVM	-	Measure vector voltmeter - HP8405A
REDACV	-	Read the ACVM Ballantine 3571
REDSWG	-	Read network analyzer - GR1710
REDVVM	-	Read vector voltmeter - HP8405A

VII. Dedicated Instrument Statements

REDPW	-	Read RF Power Meter HP432C
MONITOR	-	Monitor a power supply for a desired voltage
MONCUR	-	Monitor a power supply for a desired current

TABLE I · RATEL TEST ORIENTED STATEMENTS

- Power reset or initialize an individual instrument or the entire test station
- Prepare an instrument to apply a stimuli or to take a measurement.
- Command a measuring instrument into a continuous measurement mode
- Direct an instrument to make a reading according to its programmed preparation.

Matrix and GPR Communication Statements - a) Route stimuli and measurement signals through the test station Switching Matrix to and from the appropriate UUT pins, b) supply up to 48 bits of digital data via a general purpose register for functional testing on devices requiring DC patterns, and c) supply up to 48 bits of digital data in parallel to a UUT.

Time Readout Statements - give the UUT programmer the facility for real-time clock monitoring and for instituting program delays during execution.

Program Control Statements - cause the test station to perform unique automatic test station actions. These include the following operations:

- Terminate execution, perform finish-up functions on the unit (e.g., accept/reject decisions) and then return all station hardware to a quiescent state.
- Generate an abort condition
- Permit the execution of a program to pause and then branch a an operator response from the special function keys (Figure 5)
- Examine certain test station operating conditions (e.g., in production mode testing, current unit has a failed reading,etc.)
- Transfer control from one executing program segment to another
- Provide to the test system the starting location, test number, and total count of a test reading sequence
- Specify and permanently record numeric and bit pattern test data readings
- Retrieve classified frequencies
- Retrieve integer code value of adapter connected to a UUT

Table Processing statements - direct a communication to be made to the central system to catalog or retrieve data structures.

Non-direct Readout Statements - a few programmable measuring instruments generate outputs which exist as DC voltage levels and thus are not directly available in digital form. The RATEL non-direct readout statements determine these measurement values by programming intermediary devices to convert the DC voltages to digital patterns and then performing the necessary data manipulations and conversions to standard units of measure.

Dedicated Instrument Statements - are designed for certain instruments (such as power supplies) which must have dedicated verb type statements to program them).

UUT PROGRAM

Each UUT program is written as a completely self-contained RATEL coding module with the exception of the calls to station support routines such as the Math Library and Instrument Drivers. Instruments are programmed by specifying their programmable functions in standard engineering terminology, for example:

```
ENTER (DVM, VDC, 100)
INPUT (DVM, VOLTS)
```

Execution of the ENTER statement prepares the digital voltmeter to take a DC voltage reading on the 100 volt scale. Execution of the INPUT statement causes the Digital Voltmeter to actually perform the read action and return the value in the variable VOLTS.

Programs are initially created via cards and entered onto Central's disk from the card reader. An alphabetic revision and numeric compile count identify every program statement. During program generation and investigation, unlimited program modifications can occur with each generation identified by a unique compile count. Program revisions are also associated with production serial number effectivities for the UUT. UUT programs have the following characteristics:

- Programs are named from the production control part number assigned to the unit.
- Comments are allowed on each statement line as well as in Comment statements
- The user can generate his own assembly language procedures for referencing by the UUT program.
- Symbolic names may be any length for the programmers convenience with the first five characters being unique (characters after the first five are ignored).
- The Central disk is accessable during program execution for retrieving and cataloging data areas

STATION SUPPORT SOFTWARE

Each station Process Controller is software controlled by an Executive program called "MONITOR/TASK MANAGER". Activating the test station via the bootstrap load brings in the Executive program. The "MONITOR/TASK MANAGER" responds to the mode selection made by the user/operator to bring into core from the Central System the desired support system or test program. To manage test program execution, a Run Time System Interpreter is included as part of the UUT program sent from the Central. Support systems include a Compiler and Editor for program maintenance and special software to assist in station maintenance.

Since a significantly large variety of units are being tested, every effort is made to minimize program generation, validation, and execution time. A RATEL source EDITOR gives a programmer the interactive capability via the Keyboard/CRT to perform on-line maintenance support for any UUT program. The EDITOR performs program displays, selective statement displays, and maintenance activity (adds, changes, deletes) resulting in program modifications. It also locates all references to a given character string within a selected program unit. During program validation, an online Trace option helps the user follow the program path and the computation of values by printing information about program identifiers (value of variables, DO loop parameters) and structure points (all branch labels and subroutines entered/exited). The user enters and exits the Trace mode at will, via the Keyboard/CRT. (ATTENTION option).

CONCLUSIONS

The Distributive Intelligence Factory Test System being used in the manufacturing process of SAM-D electronic assemblies has been in daily operation since 1973. The SAM-D Missile system is currently in the Engineering Development phase which precedes the Production and Deployment phases (5). The test complex described here supports the eight stations used in the SAM-D Development phase. Initial launches from White Sands Missile Range have been a "Resounding Success" (6,7). Just recently, (8), an important flight test was "Impressive". It is projected that as requirements for specific test functions expand and the test work load increase, more test stations will be designed and ultimately integrated into the test complex.

On closing, it should be noted that while the test system is currently being used to test SAM-D assemblies, its capabilities could be extended as a factory test system in other application areas.

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PERSHING Ia TEST EQUIPMENT

J. Frank Dement

Martin Marietta Aerospace

Orlando, Florida 32805

ABSTRACT

Pershing Ia maintenance philosophy is described, followed by functional descriptions of selected pieces of test and checkout equipment for use in forward area, rear area, and factory test and maintenance work. Normalized cost data and cost drivers are presented and two manufacturing technology projects are proposed.

INTRODUCTION

This paper, which was prepared for the Army Materiel Command Missile Manufacturing Conference, Test Equipment Panel, describes the Pershing Ia (prior to addition of the Automatic Reference System and the Sequential Launch Adapter) missile system.

Major missile systems such as Pershing have a large number of pieces of test and checkout equipment. Therefore the test equipments described here were selected so that each major area of use would be represented by a major piece of equipment.

THE PERSHING WEAPON SYSTEM

The Pershing Ia Weapon System is a tactical, mobile ballistic missile system possessing the capability to respond effectively to any nuclear or major nonnuclear threat to the United States or its allies.

The system is comprised of all firing battery components required to conduct launch operations as well as equipment necessary for rear area support and maintenance functions. Firing battery autonomy is the keynote requirement.

In its basic scenario, the missile delivers a nuclear warhead to a preselected target out to a range of 400 miles from the launch point (Figure 1). When the missile is fired, the first stage rocket motor is ignited, Pershing liftoff occurs and the missile begins a predetermined pitchover maneuver toward the target. When first stage burnout is achieved the missile enters a coast period. At the end of the coast period, first stage separation occurs and the second stage rocket motor is ignited to accelerate the remaining missile sections along the flight path. During second stage burn, the guidance computer constantly computes the missile's velocity and displacement. When the proper values of attitude, range, and velocity have been attained a thrust termination signal is applied, second stage separation occurs, and the warhead is spun at 32 rpm to stabilize its forward motion as it continues on a ballistic trajectory to the target.

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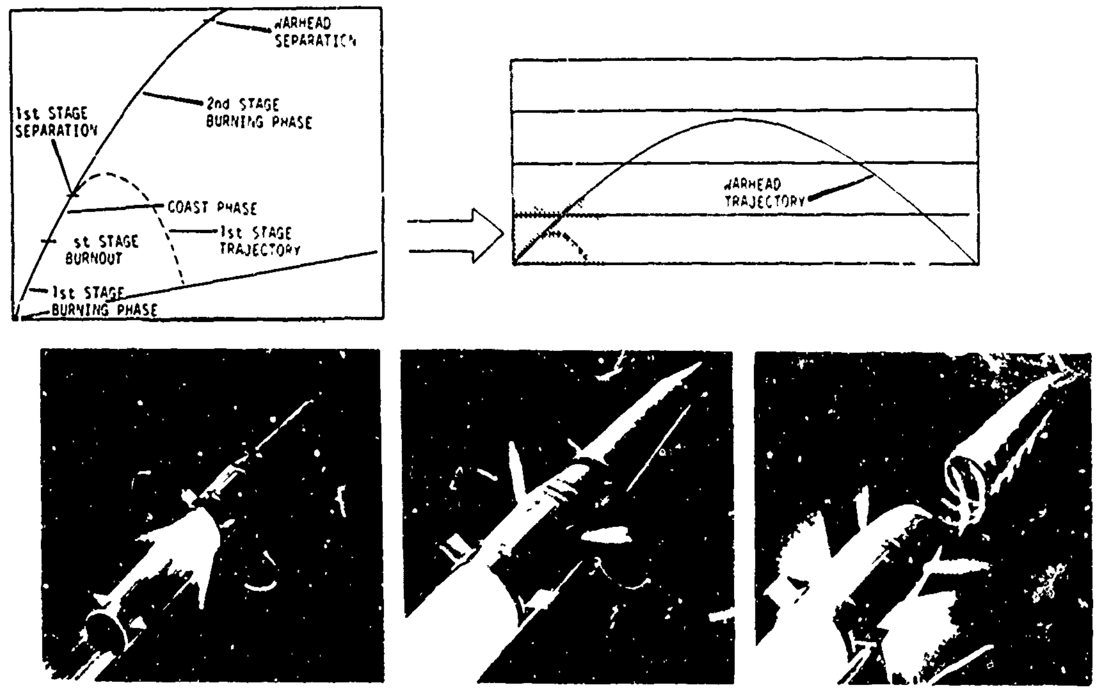


First Stage Separation *Warhead Separation* *Warhead Spinning for Stabilization*

Figure 1. Typical Pershing Flight Scenario

Pershing Ia Firing Battery Components

The various components required to conduct launch operations at the firing battery are the missile, erector-launcher, programmer-test station and power station, azimuth laying set, battery control central, and the radio terminal set. The latter two devices are utilized to maintain communications with higher headquarters so as to control and coordinate firing battery operations. All of these components are mounted on wheeled vehicles (Figure 2) except for the azimuth laying set which is transported on a 2 1/2 ton cargo vehicle and unloaded for use.

Missile. The Pershing missile is a two-stage, surface-to-surface ballistic weapon capable of engaging targets out to 400 miles. It has an all-inertial guidance system which places the nuclear warhead in a preselected ballistic trajectory by using data inserted into the guidance and control computer before liftoff. Once the missile is airborne, it is completely free of ground control and therefore unaffected by all known methods of guidance countermeasures.

Erector-Launcher. Designed for simplified transportation and fast erection and firing of the Pershing missile, the erector-launcher is capable of paved road or cross country travel. At the firing site automatic erection and leveling contribute to a very rapid rate of fire. The erector-launcher (EL) with missile aboard is towed by the XM757 tractor. The erector-launcher (EL) with missile aboard can also be transported by C-130, C-133, and C-141 aircraft.

Programmer-Test Station and Power Station. The programmer-test station (PTS) is carried on an M656 vehicle and features solution of firing equations, rapid missile checkout and countdowns, with complete computer control, and automatic self-test and malfunction

isolation. Additionally, the PTS performs tests that simulate airborne missile operation, programs the trajectory of the missile, and controls the firing sequence. The power station, which provides the primary electrical and pneumatic power for the missile and ground support equipment at the firing position, is transported on the same vehicle.

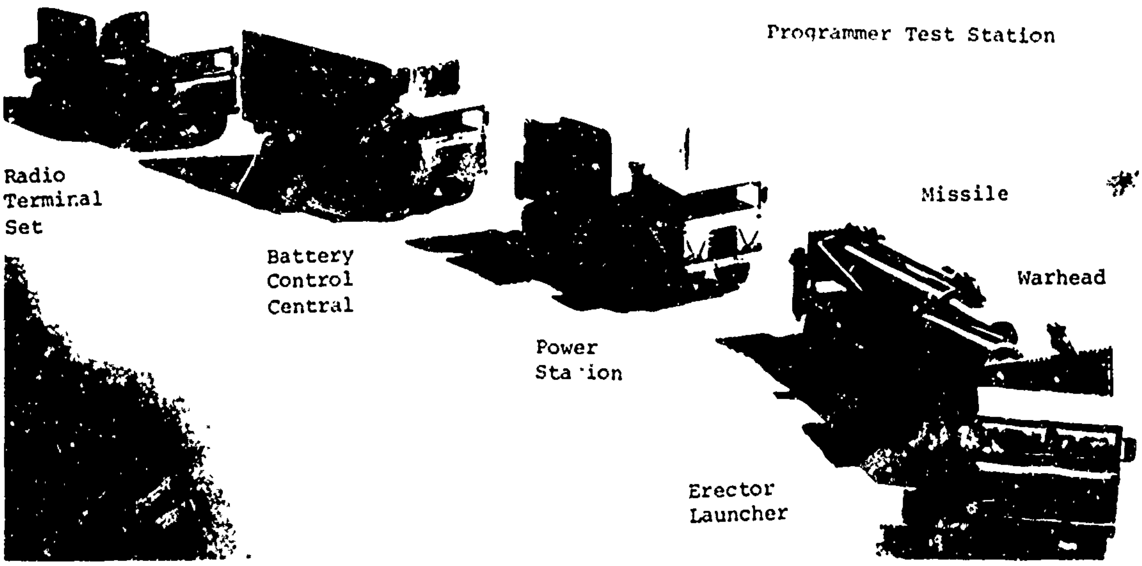


Figure 2. Pershing Ia Firing Battery Components

Rear Area Support Components

All elements of the system are maintained in a state of combat readiness by the rear area support equipment.

The system components test station (SCTS) is used to perform rear area maintenance of the Pershing system (Figure 3). Housed in a mobile center, the SCTS under computer control tests missile sections and assemblies, cards, relays, and modules from the guided missile and associated ground support equipment. Diagnostic programs are also provided for verification and troubleshooting of major SCTS assemblies. The SCTS contains a dismounted PTS and has facilities whereby one missile guidance section can be tested and another repaired simultaneously under controlled temperature conditions. Power for the SCTS originates from the power station equivalent.

The power station equivalent (PSE) provides the same outputs as the firing battery power station but is capable of more sustained operation. Comprised of two trailer-mounted power stations and one facilities-distribution trailer (Figure 4), the PSE furnishes all the power required for rear area checkout.

Several shops and semitrailer vans (Figure 5) are assigned to the rear area to provide facilities for electrical and mechanical maintenance and repair, parts storage, and offices for direction and control of direct support and general support maintenance functions.

Separate reusable shipping and storage containers (Figure 6) are provided for each of the four missile sections. The containers protect the missile sections from the effects of excessive vibration, abnormal handling, and intolerable atmospheric conditions.

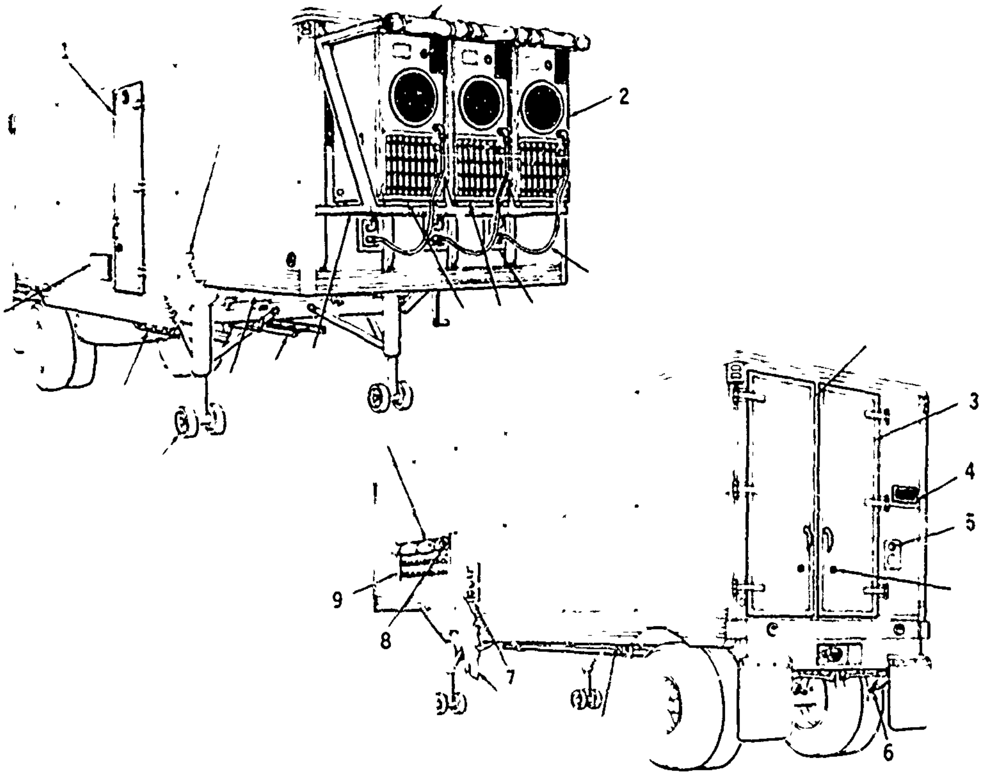


Figure 3. System Components Test Station Exterior View

1 - Personnel door
2 - Air conditioner-heater
3 - Eq.'pment entrance door (2)
4 - Air vent filter
5 - Humidity indicator
6 - Leveling jack (2)
7 - PTS power cable entry panel
8 - Safety lanyard
9 - SCTS main cable entry panel
- Modification mounting panel

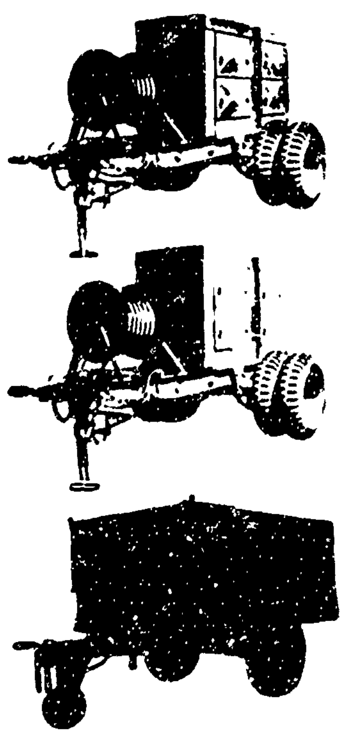
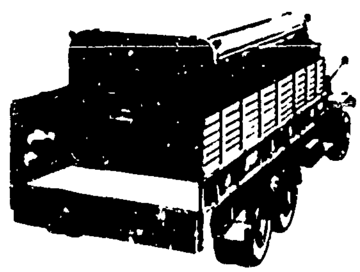


Figure 4. Power Station Equivalent

Maintenance Shop



Repair Shop

Supply Van

Figure 5. Support Shops

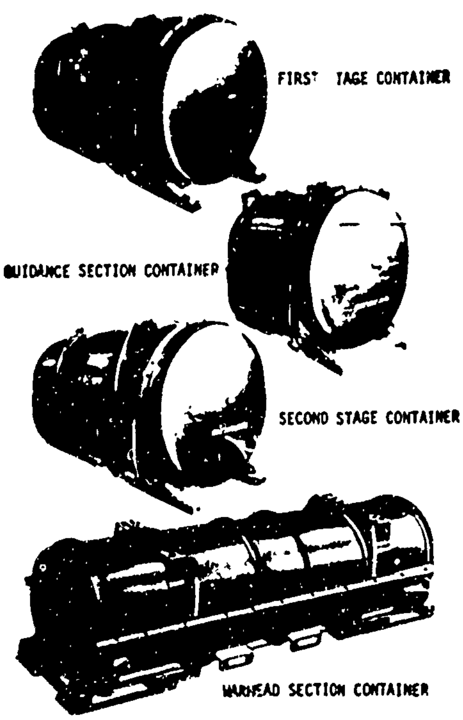


Figure 6. Missile Section Shipping and Storage Containers

Pershing Maintenance

The maintenance of the Pershing Weapon System is broken down into three areas of concern: Forward Area (firing battery), Rear Area, and Depot.

In the forward area the PTS is programmed to accomplish a self-test routine to verify its functional integrity prior to a missile countdown. During a missile countdown fault detection is accomplished automatically by the PTS. In the case of a missile failure, corrective maintenance is accomplished by the replacement of the defective missile section. Upon detection of a PTS failure during countdown, the countdown program will callout a diagnostic tape program which will fault isolate the PTS to the failed subassembly. PTS

power station and erector launcher fault detection is accomplished through the use of manual testers and selfcontained panel indicators.

Rear area maintenance is accomplished mainly with the SCTS which is augmented by a complement of tools, test equipment and repair facilities contained in special shop sets.

Missile section and subassembly test, fault detection, and isolation are accomplished in the SCTS. Section corrective maintenance is limited to assembly replacement. Missile assemblies are functionally verified in the SCTS and the missile guidance and control computer is fault isolated to replaceable plug-in subassemblies. All other missile subassemblies are repaired at depot.

Self-test tape program routines are periodically conducted to verify the SCTS functional integrity. Upon detection of a fault, special diagnostic tape programs are called out which will fault isolate the respective SCTS assembly. Corrective maintenance consists of replacement of defective assemblies, subassemblies, cards, relays, test connectors, cables and wiring.

Depot maintenance functions encompass the capability of the field and the manufacturer. The depot has the facilities for overhaul, repair and test of components using tools and test equipment similar to, or the same as those used in the factory.

The Programmer Test Station

The programmer-test station (PTS) functions as a mobile fire control center for the Pershing system. PTS equipment controls prelaunch and launch sequences, computes missile presets and firing azimuth, and provides communications, power distribution, and control. The PTS also provides basic test and malfunction analysis, including fault isolation and self-test capabilities. The primary operating circuits of the PTS are contained in three groups of functional equipment: a console, a computer, and an adapter (Figure 7). The console is used for the following: manually entering information into the computer; initiating, controlling, and monitoring the firing sequence; and performing fault isolation procedures. From the console, the operator applies power to the computer and adapter, enters the program for the fire sequence, and enters the data (manual data entry) pertaining to the firing position location, the target location, and the type of warhead burst. Command signals, digital in format and properly programmed by the computer, are applied to the adapter. The adapter either converts these signals into analog signal voltages or buffers them for use in presetting the missile guidance section, monitoring and controlling the operation of the ground support equipment, and checking the missile sections when in containers. In addition, the adapter converts monitor and command signals from the missile, ground support equipment, and missile sections in containers and sends them to the computer for analysis and to the console which indicates the status of the fire sequence.

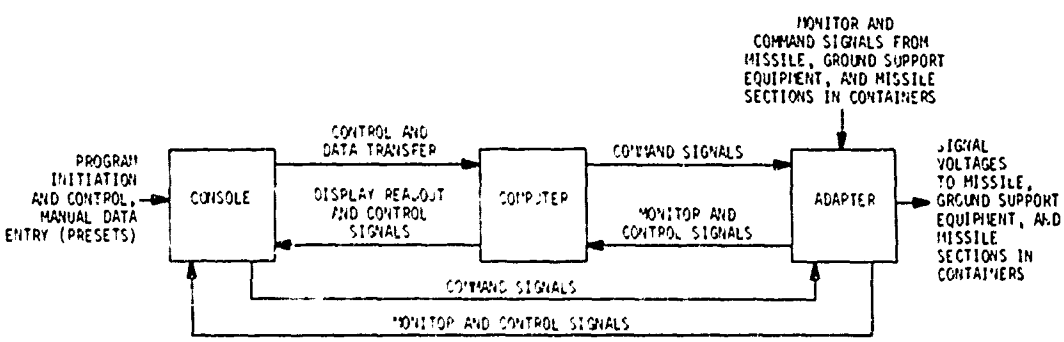
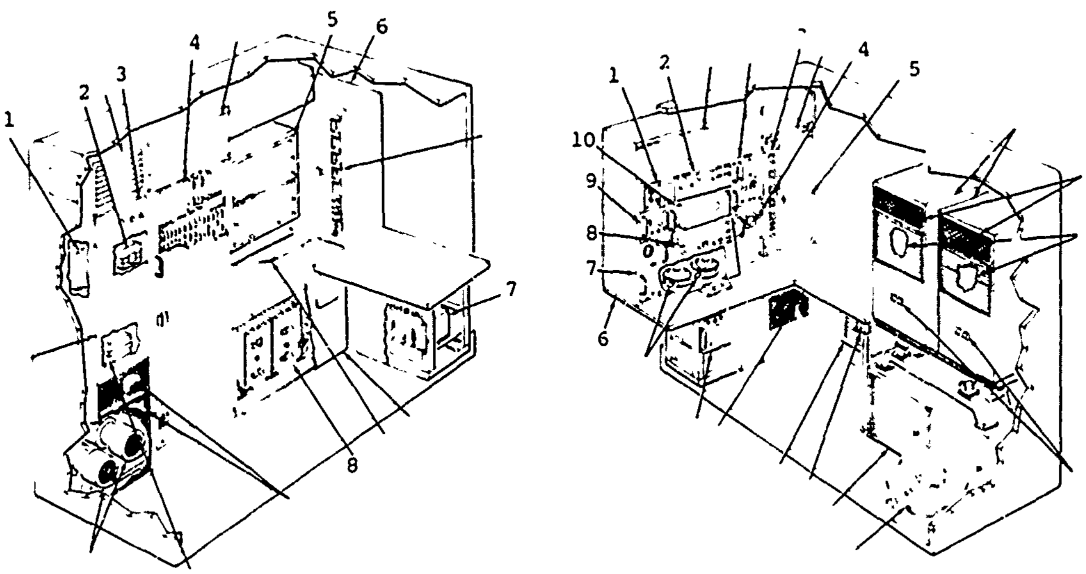


Figure 7. Programmer Test Station Block Diagram

The PTS is housed in a shelter constructed of foamed-in-place panels. The basic shelter is approximately 7 feet high by 8 feet long by 7 feet wide. There are four isoskids, one on each corner, for shelter protection in case it is accidently dropped. Five cable entry panels provide access to all cable connections. The arrangement of the

interior of the PTS shelter is shown in Figure 8. The operators console is composed of a number of panels which contain the switches and displays used by the operator. The countdown panel, the tape reader, and the maintenance panel are considered to be functionally part of the computer. The remaining panels include the utility panel, the azimuth laying control panel, and the phone control-voltage monitor panels.



Left Side View

1 - REMOTE FIRING BOX
2 - AZIMUTH LAYING CONTROL BOX
3 - PHONE CONTROL PANEL ASSEMBLY
*4 - ADAPTER
*5 - CARD AND MODULE TEST SET
*6 - POWER DISTRIBUTION ASSEMBLY
*7 - SIGNAL DISTRIBUTION BOX
*8 - COMPUTER

Right Side View

1 - LAUNCH CONTROL PANEL ASSEMBLY
2 - MAINTENANCE PANEL ASSEMBLY
*3 - UTILITY CIRCUIT BREAKER PANEL ASSEMBLY
4 - TELEPRINTER
5 - TAPE STORAGE CABINET
*6 - CONSOLE
7 - VOLTAGE-PHONE MONITOR PANEL ASSEMBLY
8 - COUNTDOWN CONTROL PANEL ASSEMBLY
9 - AZIMUTH LAYING CONTROL PANEL ASSEMBLY
10 - TAPE READER

*COMMON TO PTS/SCTS

Figure 8. PTS Interior View

The controling and sequencing element in the PTS is a general-purpose computer. The computer is a stored program, parallel, binary, fixed point machine, whose major components are a central data processor, an input/output assembly, four core memory units, a power supply assembly and an electrical equipment rack assembly. The basic word length is 23 data bits plus sign and parity (25 bits total). The memory is magnetic core, random access, with a 4 microsecond cycle time. The computer is normally supplied with 16,384 words of memory capacity, but can be expanded without redesign. The computer employs 45 basic instructions, but by using microprogramming techniques, up to 300 instruction variations are available to the programmer. The memory is protected so that accidental interruption of input power to the computer will not cause the contents of the memory to be altered. The input and output circuits of the computer are compatible with devices using field data codes. A simplified block diagram of the computer and control console is shown in Figure 9.

The control console provides the controls and indicators by which the operator controls and monitors the operation of the PTS. From the console, the operator controls the application of power to the adapter and the computer, enters data, and observes indicators that display the status and condition of the fire sequence. The console contains the azimuth laying control panel assembly, voltage-phone monitor panel assembly, maintenance

panel assembly, tape reader, countdown control panel assembly, utility panel assembly, teleprinter, and launch control panel assembly, utility panel assembly, teleprinter, and launch control panel assembly.

The countdown control panel assembly is used for manually entering data into the computer during program execution. A visual display indicator on this panel indicates which phase of the program is in progress, the reason for hold conditions when a hold condition exists, and the cause of a malfunction when a malfunction occurs.

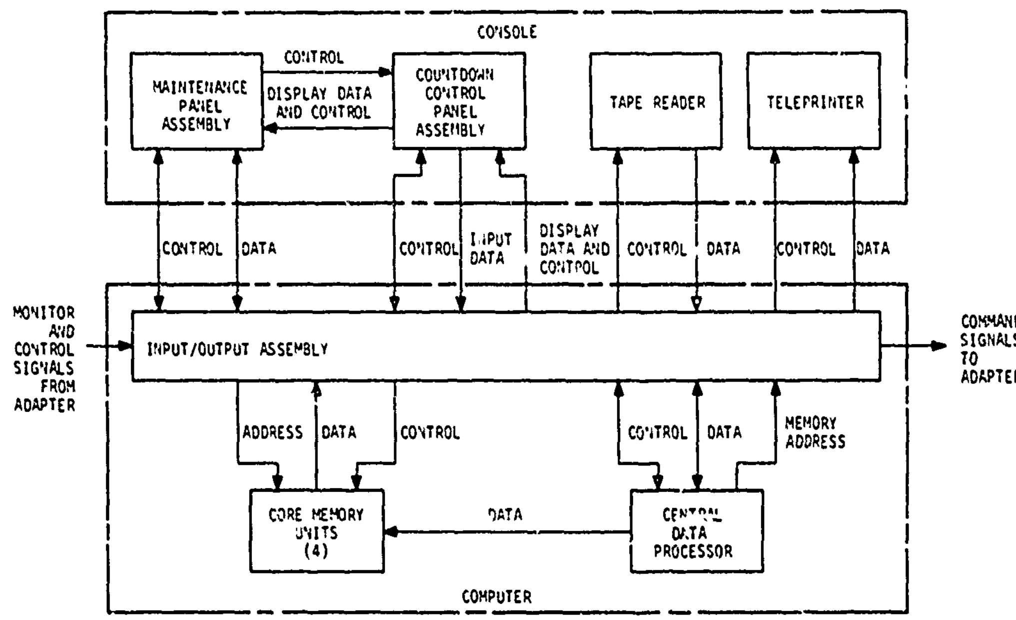


Figure 9. Computer and Control Console Block Diagram

The tape reader is used for entering punched tape program data into the computer.

The teleprinter provides a historical record of all data and all information displayed on the countdown control panel assembly information readout indicator during a fire sequence.

The maintenance panel assembly is used in conjunction with prepunched diagnostic tape when fault isolation procedures are being performed on the computer. It contains three alphanumeric display tubes. A number is displayed for each step of the test. Comparison of the number displayed with similar numbers in the repair data tables results in isolation of the malfunction.

The adapter serves as the electrical interface between the computer and t' missile system. All electronic circuits of the PTS which are not part of the computer, the utility circuits, or the console equipment are included in the adapter (Figure 10).

Operating under the control of the computer, the adapter circuits perform most of the actual controlling and monitoring function of the PTS. There are 215 control lines which can be switched on and off by the computer through adapter circuits: this number can be increased to 360 without basic design changes. An additional 215 lines are monitored for the presence or absence of signals; this number can be increased to 396 without basic design changes. The adapter accepts digital information from the computer in the form of an 18-bit parallel word, converts this information into analog information or buffers

digital words for presetting the guidance system and sequencing the countdown of the missile for flight. Circuits within the adapter also convert analog information from the card and module test set (CMTS) and the ground support equipment to digital information for the computer.

The adapter circuits consists of 70 printed circuit cards (18 different types) and 231 modules (5 different types). The modules are plugged into the register board and the printed circuit cards are contained within the electrical equipment rack.

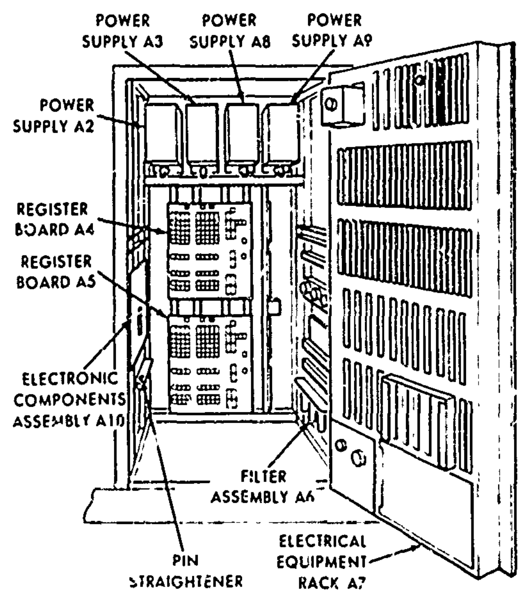


Figure 10. Adapter Assemblies

The functions and interfaces of the adapter are shown in Figure 11. The operations and control function, using reset, row select and data from the computer, generates the command signals necessary for the operation of the adapter, the CMTS, the azimuth laying equipment and the console. This function also generates echo signals to the computer on completion of a function.

The command and monitoring function, on command from the operations and control function, produces control signals for use by and monitor signals from the missile, ground support equipment and the CMTS. Status is provided by this function to the control panel and the remote fire box.

The platform alignment function, in conjunction with the azimuth laying equipment, aligns the missile platform. This function is controlled by the operations and control function.

The ac/dc stimuli function, under computer control, generates the necessary stimuli for platform alignment, command and monitoring, measurements and presetting functions. It also supplies stimuli to the missile, ground support equipment, CMTS, and missile sections in containers.

The measurements function, under computer control, measures ac/dc voltage, frequency, and makes phase comparisons.

The card and module test set (CMTS) operates automatically in conjunction with the computer and adapter to test the cards and modules of the adapter, the CMTS, and the circuit network modules of the computer. Operating under computer control, the CMTS connects

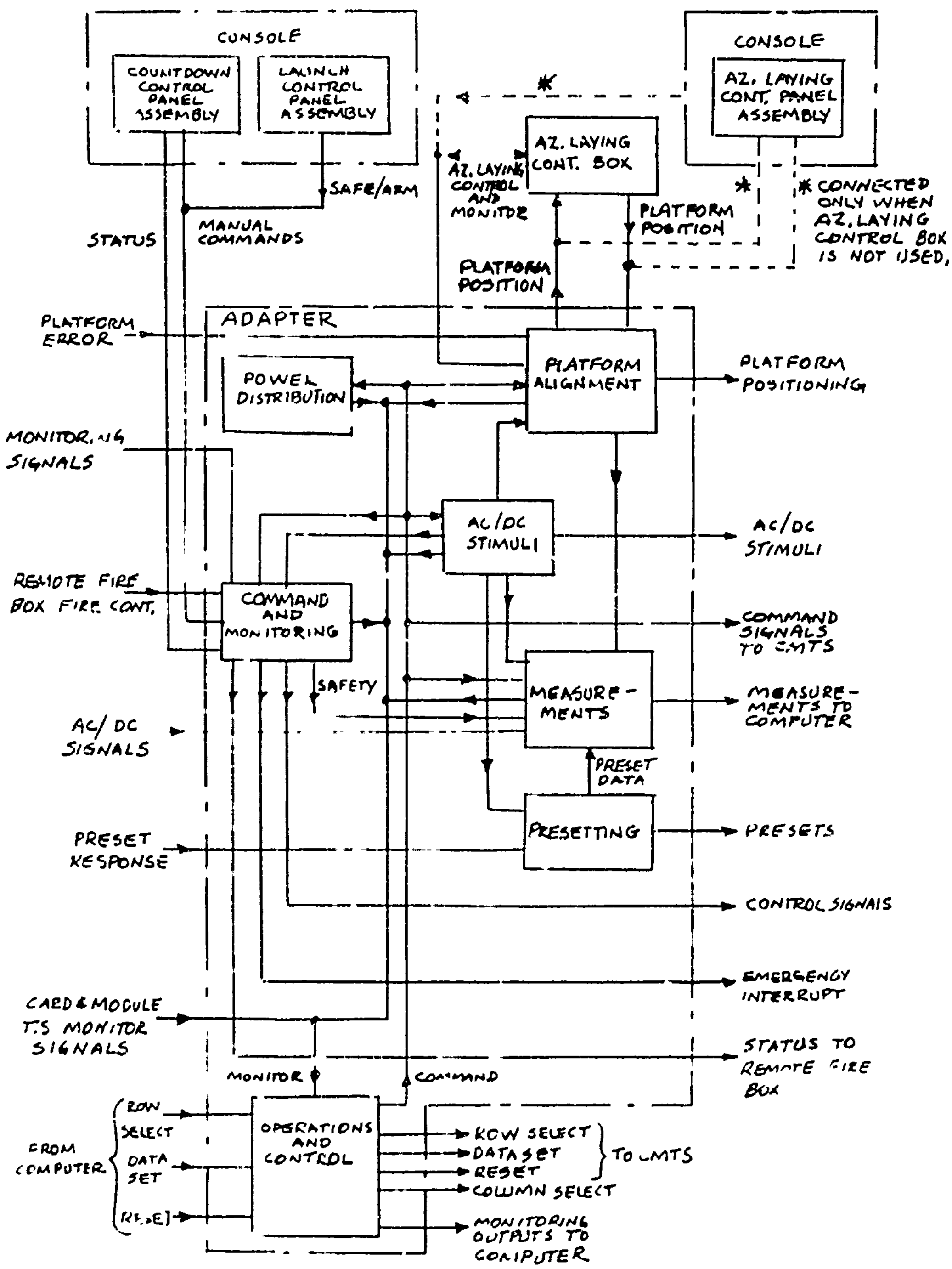


Figure 11. Adapter Function Block Diagram

power, internally generated stimuli, and adapter-generated stimuli. Any test loads required are also connected. The CMTS monitors and measures the circuit outputs and the results are sent to the computer. The computer compares the results with predetermined standards to determine whether or not the circuit outputs are within prestored tolerance. If they are not, the test is halted and the readout of the failure test is displayed.

System Components Test Station

The system components test station (SCTS) is used in performing rear area maintenance of the PIa system. It utilizes a computer and tape programs for testing missile sections and assemblies, cards, relays, and modules from the guided missile and associated ground support equipment. Diagnostic tape programs are also provided for verification and troubleshooting of major SCTS assemblies. The SCTS contains a dismounted PTS and has facilities whereby one missile guidance section can be tested and another repaired simultaneously under controlled temperature conditions. The major assemblies of the SCTS are divided into two categories: PTS assemblies and SCTS assemblies (Figure 12).

<u>PTS Assemblies</u>. The major PTS assemblies used in the SCTS are the adapter, card and module test set, power distribution cabinet, console, computer, utility circuit breaker

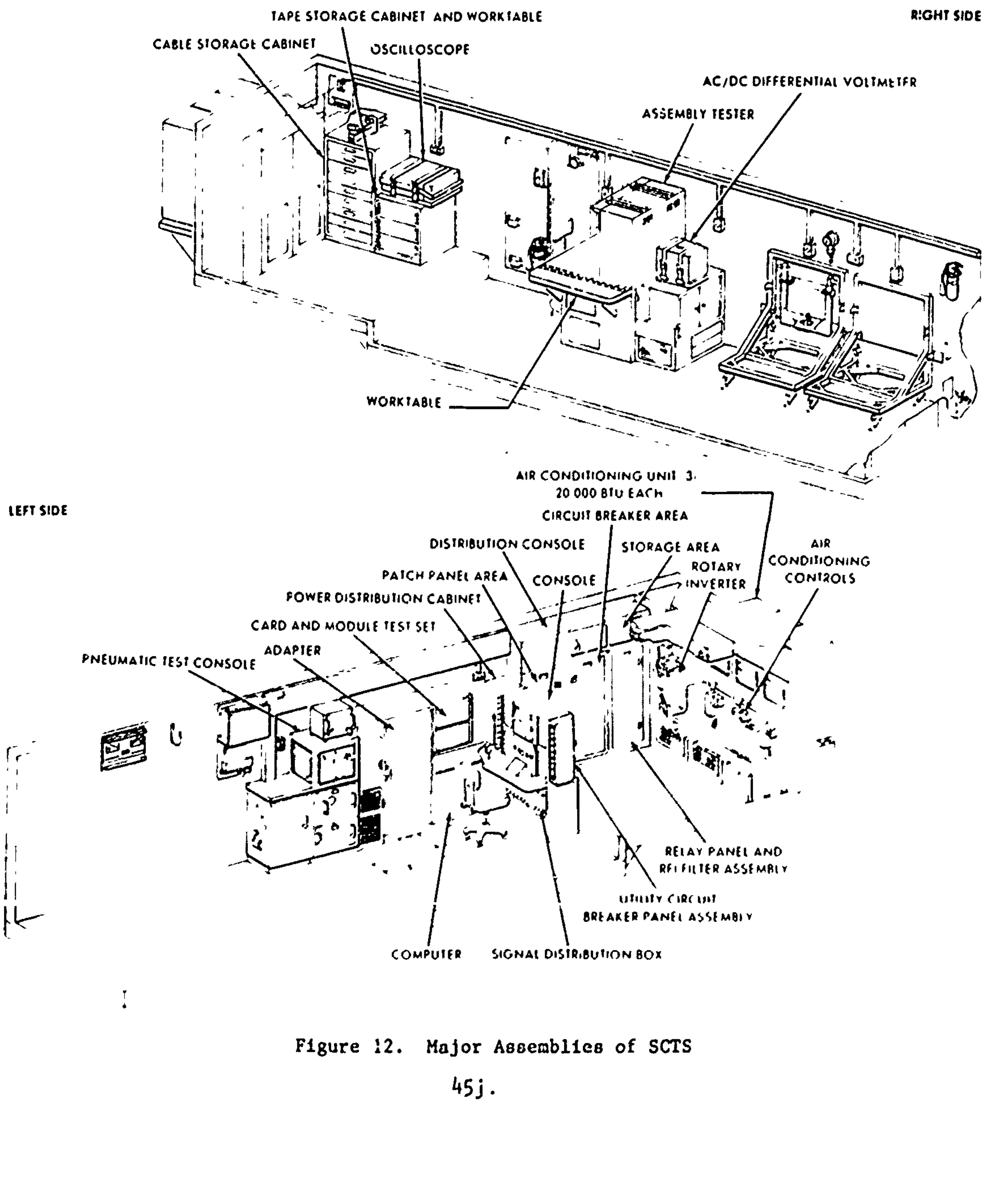


Figure 12. Major Assemblies of SCTS

panel assembly, and signal distribution box. The PTS assemblies are used when testing missile sections, PTS circuit cards, and PTS modules. These assemblies perform the same functions as in the PTS.

SCTS Consoles and Assemblies. The major SCTS consoles and assemblies are pneumatic test console and assembly tester (Figures 13 and 14). Other significant assemblies of the SCTS are the distribution console, the cable and tape storage cabinets, oscilloscope, and ac/dc differential voltmeter.

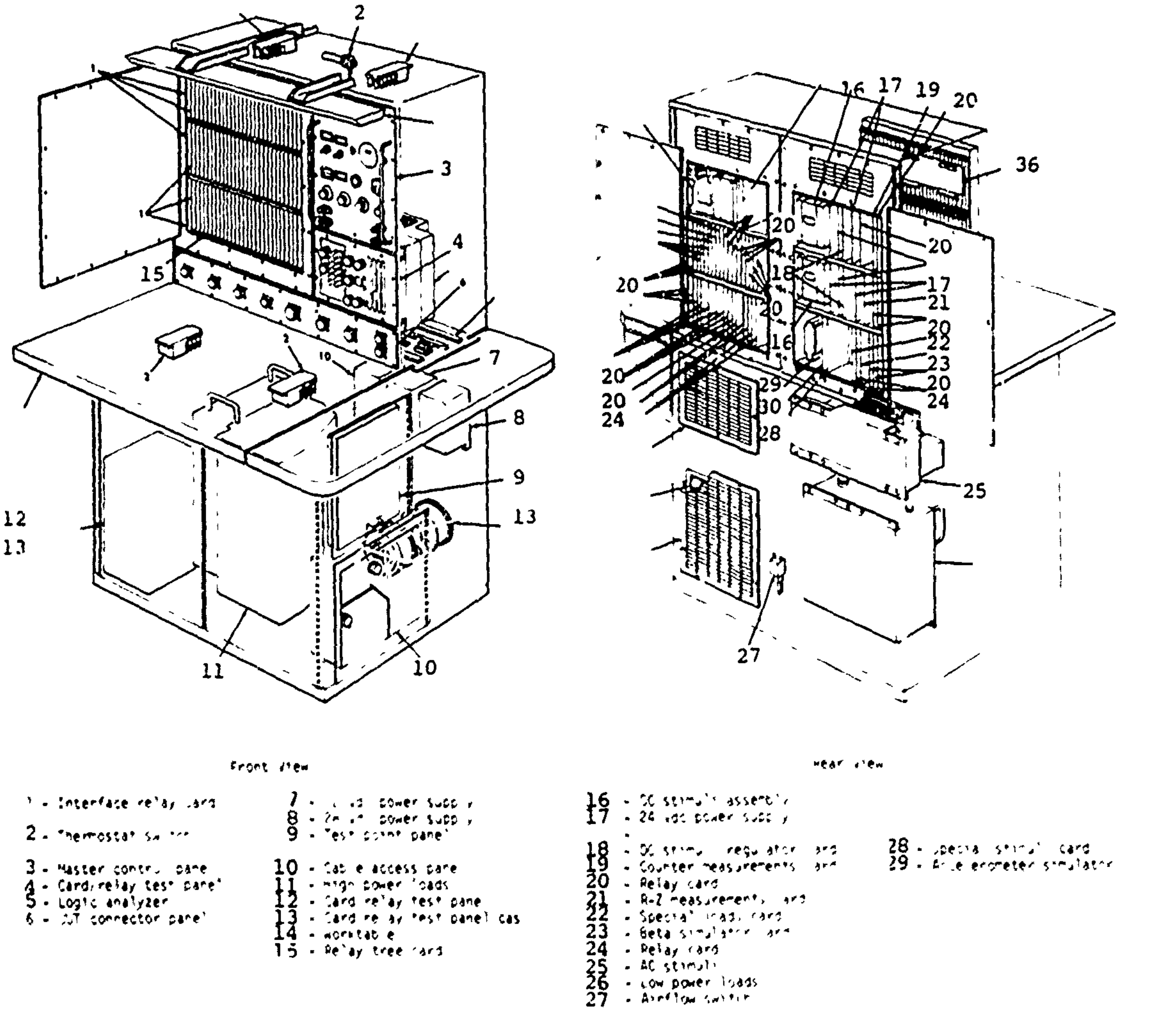


Figure 13. Assembly Tester

The distribution console distributes primary power to all SCTS major consoles and assemblies within the SCTS van. In addition, it routes test signals to and from the missile sections under test. The distribution console contains a patchboard receptacle, a circuit breaker panel, a relay panel, radio frequency interference (RFI) filters, and a storage area for technical manuals.

A rotary inverter supplies precise 115 volt, 3-phase, 400 Hz power to the assembly tester and to the applicable UUT's on the assembly tester.

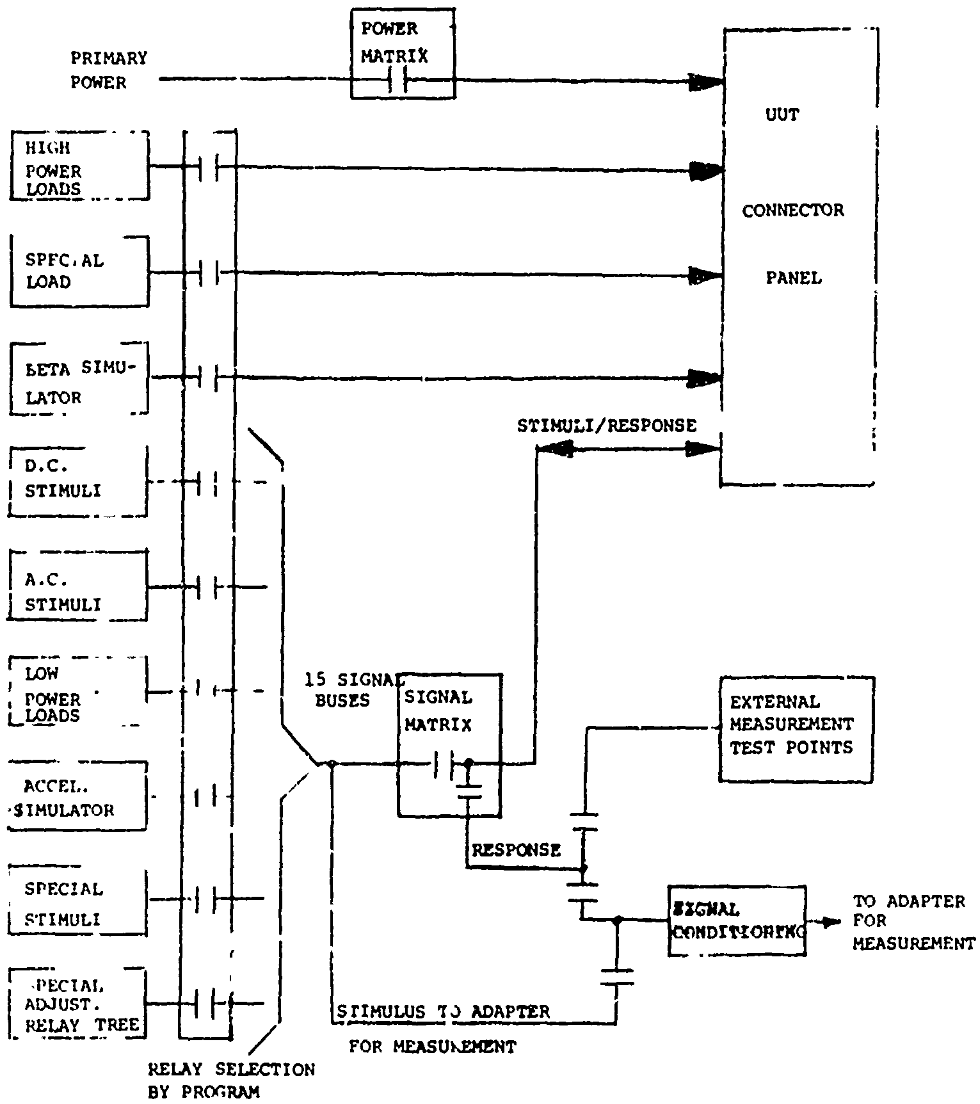


Figure 14. Block Diagram Assembly Tester

The air conditioner-heater control panel is used to set the air temperature output of the air conditioner-heaters. The air conditioner-heaters supply either cool or warm air as required to maintain the interior at a temperature of 77°F ±6°F.

Storage cabinets are provided for the UUT cables and programmed tapes used during assembly tester checkout of a UUT.

An oscilloscope and an ac/dc differential voltmeter are used during UUT testing when adjustments and critical voltage measurements are required. The are also used for fault isolating and troubleshooting the assemblies within the SCTS.

The assembly tester provides necessary stimuli, loads and switching operations for functionally testing certain assemblies, printed circuit cards, and relays of the Pershing weapon system. Programmed by row and column select signals from the adapter, the assembly tester performs essentially three functions in the following order: generation of the

required stimuli and loads, application of the selected stimuli and loads to the unit under test (UUT) and preparation of the UUT responses for measurement by the adapter and computer.

Stimuli and loads selection is accomplished, under computer control, through relay matrix controlled interface relays to signal buses or to two special connectors on the UUT connector panel. Most of the buses are time shared. From the signal buses, stimuli and loads can be routed to signal routing function for application to a UUT or to signal measurement function for verification of proper value.

A signal matrix consisting of 75 relay tree cards can switch functions to any one of 150 pins on three UUT connectors. The matrix switches stimuli and loads to the UUT and routes the UUT response to the signal measurement function where the signal is digitized for comparison to preprogrammed tolerances.

The digital logic analyzer (DLA) is used in conjunction with the assembly tester to test and fault isolate the guidance and control computer (G&CC) as a UUT. Under program control, the DLA is capable of loading a 16-bit binary word into the G&CC registers and memory-controlling the starting of the G&CC central processor; simulating G&CC input-output control functions; testing the G&CC input-output bus, address bus and the communication signals, and monitoring the logic levels of preselected signals generated in the G&CC.

The pneumatic test console (Figure 15) performs tests on the guidance section platform air supply system when the guidance section is mounted on the test dolly inside the SCTS van. It also tests the ability of the guidance section to remain pressurized during flight. The replaceable items in the platform air supply system that can be tested are the pressure switches, air pressure regulator, heater, and heater thermostat. The high-pressure air supplied by the pneumatic test console is also used to precharge the hydraulic actuators, if required, during their UUT testing.

Software

The forward area software used in the PTS consists of fourteen major tape programs. These tape programs are countdowns, diagnostics, missile sections, and trainers.

The above tapes are batch processed with a large data center computer using an assembly program. The assembler program is a FORTRAN program which will accept the three levels of language used (D84 symbolic, Pershing symbolic and D84 Octal) to produce the software. The D84 symbolic is an interpretive language on a one for one command. The Pershing symbolic is a special language that allows the program to call on subroutines after being decoded by an executive subroutine. The D84 Octal is strictly machine language code.

The rear area software used in the SCTS consists of twenty-four major programs. These programs are used for diagnostics, UUT testing and calibration. The above programs are developed by the use of a FORTRAN Assembly program which is processed at a Data Center. The assembly program accepts input of a special language (SCTS) which was developed for rear area programming. It controls I/O drivers used during the UUT testing. Forward and rear area programs are documented and punched on mylar tape.

Scope of Software

Forward Area (PTS)	Rear Area (SCTS)
Fourteen Major Tape Programs	Twenty-four - Major Tape Programs
1. 3 countdown programs	1. 2 executive
2. 2 diagnostic programs	2. 2 airborne loader
3. 2 missile section	3. 2 diagnostic
4. 2 middile in-container	4. 17 UUT master tapes 130 individual programs
5. 2 trainer	
6. 2 card test UUT	5. 1 calibration
7. 1 computer diagnostic	

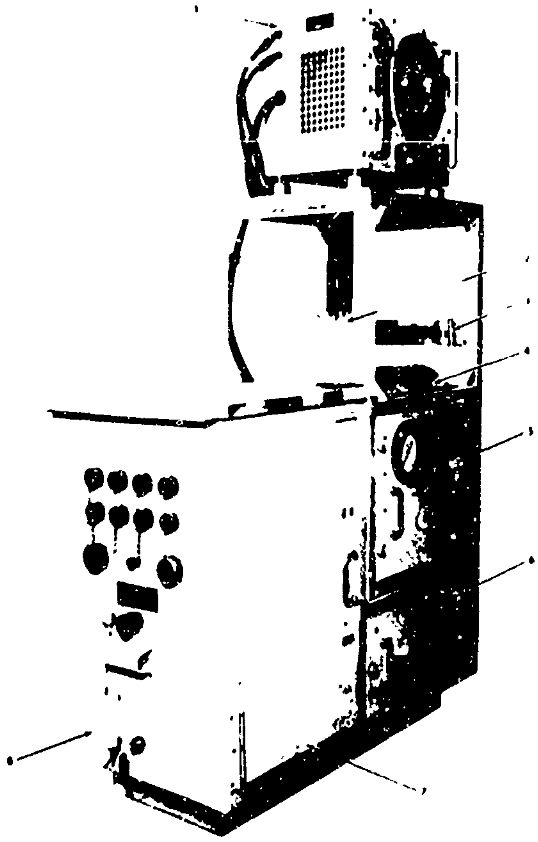


Figure 15. Pneumatic Test Console Assemblies

1 - Pressure test set	5 - Pneumatic test chassis
2 - Pneumatic chamber	6 - Storage drawer
3 - Hand pump	7 - Storage cabinet
4 - Pneumatic control panel	8 - Connector panel

Acceptance Testing, Pershing

Factory (acceptance) testing of the Pershing system is for the most part performed using manually controlled equipment. An example of this is the test equipment at control point 713 where full up guidance sections are tested.

Tests are limited to those functions which interface with other items; e.g., other missile sections and the ground support equipment. A complete test of a "go" G&C section requires two men and 32 hours.

The guidance and control section test set at control point 713 serves to confirm that the assembly of components previously tested at the subassembly level does, in fact, function correctly as a complete subsystem. It also assures the success of subsequent electronic and mechanical marriage of the G&C section with the other missile sections and with its tactical ground support equipment. To most efficiently meet these objectives, the design of CP713 test equipment is based on a philosophy which restricts the test interface to those input-output parameters affecting marriage and/or identifying problems to a black-box, or component level, using conventional troubleshooting practices. The G&C section test set consists of a group of test consoles working in conjunction with a turn-tilt-table test stand on which the section-under-test is mounted. The test consoles are used for the following major functions: operating power supplies and miscellaneous monitors, guidance and control test and evaluation, and turn-tilt table control. The operating power supplies and miscellaneous monitoring console group (three consoles) provides for both electrical

power and hi-pressure nitrogen distribution, monitors continuously, and as required, various electrical voltage (both ac and dc), contains driver amplifiers for the recorder galvanometers and a control actuator simulator. The guidance and control test and evaluation console group (four consoles) provides for control and monitoring of the guidance section test and contains a mixture of standard and special purpose test equipment designed to provide a stimuli, control, sequencing, monitoring and recording capability to fully exercise, test, and fault isolate to the component level. It provides for the performance of both static and dynamic tests and functions principally under manual control of the operator. To preclude damage to the equipment under test, to synchronize application of stimuli, and to provide for correlation of critical output data, a limited number of sequencing operations use a hard-wired programmer. The third, and final group of test equipment is the turn-tilt table controller and consists of one console. Its function is limited to control and monitor of the mechanized mount for the G&C section.

CP713 DETAILED HARDWARE DESCRIPTION

Operating Power Supplies, Monitoring Group

The operating power supply monitoring console group contains the following equipment:

1. Nitrogen Panel - Provides for automatically controlled, regulated and monitored hi-pressure nitrogen supply for inertial platform air bearings and critical cooling applications within the G&C section.

2. Noise Analyzer Panel - Provides for a continuous monitoring of the guidance and control computer output lines to detect out-of-tolerance noise conditions.

3. Voltrip Panel - Provides for a continuous monitor and alarm system for the on-board 3-phase inverter power supply voltages. In addition, it provides for manual measurement of phase-to-phase voltages.

4. Power Supply Panels - Provide current limited, remotely controlled direct current sources to simulate the on-board battery supplies.

5. Jack Panel - Serves as a common distribution point for all 28 Vdc power for both test and operation of the G&C section. It also provides for a pin jack monitor on every junction in the missile umbilical to permit manual test measurements to be performed.

6. Phi Monitor Panel - Consists of three manual ranging VTVM's for continuous, separate monitoring of the inertial platforms' pitch, yaw, and roll output signals.

7. Ac/dc Readout Panel - This unit is a standard NLS digital multimeter and is used to manually measure continuity and both ac and dc voltages. It can be patched into the overall system to semiautomatically indicate selected test parameters.

8. Beta Simulator Panel - Provides a simulation of both the first and second stage control surface actuators and is used to perform closed loop tests of the guidance system. Provision is also made for pickoff, conditioning and display of the computed guidance commands to the individual control surfaces.

9. Galvo Drivers Panel - The four galvanometer driver amplifiers for the analog data recorder are housed in this panel. They are normally patched into the system to condition the control actuator command and platform command signals for analog recording. Alternately, they can be patched to any signal selected for observation that is accessible on the jack panel.

10. Ac-dc Converter Panel - This unit is a commercial ac-dc converter. It is used to convert ac test signals for measurement and display by the digital multimeter.

The guidance and control test and evaluation group contains the following equipment:

1. Analog-Sequence Recorder Panel - This unit is a commercial four channel analog and 30 channel event recorder. It normally provides a permanent record of the individual command signals to the three control surface actuators as well as the inputs to the inertial platform servo loops during a stabilization test. The 30 channels of event recording capability is used to provide correlation of turn-tilt table angles and control actuator command signals. Typically, the event channels are used to monitor and record those functions involved in prelaunch preparation and simulated flight that are time critical and sequential in nature.

2. G and C Control Center Panel - Provides for integration of the control and monitor capability of the G&C test and evaluation group. In this capacity is provides for all command switching circuitry, contains monitors for all G&C supervision indicators, and provides for the set-up capability for manually troubleshooting the control computer. Selected test functions using hard-wired sequential programs are initiated from this panel and a continuous monitor of critical temperatures within the section, such as the G&C compartment temperature, is provided.

3. Inertial Platform Auto-Sequencer Panel - Provides for the automatically sequenced operation of the inertial platform during start-up, run, and shut-down operations and monitors critical parameters, such as air-bearing temperature, to insure safe and non-destructive operation.

4. Network Tester Panels - Three separate panels are provided to test the electrical harnesses of the guidance computer, the control computer, and the inertial platform. Test capability is limited to detection of excessive, or destructive voltages on harness wiring. Normal continuity testing is performed manually using the digital multimeter.

5. Guidance and Control Computer Data Panel - Contains logic to interface a test program with the guidance and control computers. Capability is provided to transmit digital data words, monitor data transmissions, display digital data and indicate sequence steps and control function status. Incidental monitoring capability to test the missile inverter power supply frequency is also provided as a part of this panel.

6. Simulated Flight Time Generator Panel - Provides for a remotely controlled variable time gate generation capability to clock the sequence of events required to perform guidance computer integrator and simulated flight tests.

7. Accelerometer Monitor Panel - Provides visual display of the three guidance channels of the inertial reference platform. Monitoring capability is continuous and interpretation is assisted by green-band markings on the meters.

8. Sequence Control Panel - Provides the necessary control switches, indicators, and electronic circuits to enable and set up the guidance computer for performance of a simulated flight test.

9. EBW Termination Simulator - Provides a means for safely monitoring the output voltages and operating times of the various exploding bridgewire firing circuits in the guidance section.

10. Platform Monitor Panel - Provides for access to all functions available on the test receptacles of the alignment amplifier (part of the test set) and the inertial reference platform servo amplifier to facilitate manual test and troubleshooting with standard test equipment.

11. Alignment Amplifier Panel - Contains an alignment amplifier identical to the tactical prelaunch unit to earth reference the platform erection and stabilization servo loops.

12. Inverter Monitor Panels - Two separate panels are provided to sample the missile inverter power supply frequency. One provides a binary coded data word to the other for comparison with a preselected set of tolerances and generates an alarm in the event of an out-of-tolerance condition.

The turn-tilt table is controlled and monitored by a single console containing one control panel. It provides for automatic or semi-automatic sequencing of a test program to appropriately exercise the Guidance Section in a routine of pitch, yaw, and roll movements.

COST DATA

Tables I thru V show the cost of components and the amount of that cost as applied to different production categories for Pershing equipment. The percent figures within the chart indicate percentage of the total equipment cost.

COST DRIVERS

Table V lists cost drivers of test equipment for Pershing Ia. From the listing it is apparent that military requirements are the principal drivers cost. Given the restraints of military requirements, it becomes extremely important to carefully study requirements versus cost during the conceptual stage of system design.

Those items that are underlined on Table V can be worked to reduce costs.

TABLE I

Pershing PTS, SCTS and CP713 Composite Costs

	PTS (percent)	SCTS (percent)	CP713 (percent)
Simulators	-	-	33
Data processors	50	28	-
Software	-	-	-
Displays	1	1	5
Printed circuits	23	38	21
Cables/harnesses	7	13	15
Power Supplies	2	4	6
Enclosures	7	7	-
Racks	3	3	9
Environmental control	2	2	-
Documentation	-	-	-
Comm test equipment	-	1	7
Final assembly and test	6	4	4

TABLE II

Test Equipment Cost Elements
PTS

Cost Element Subsystem	Material	Parts	Fabri-cation	Assembly	Inspection	Support	Percent Production Cost
Hardware							
Stimuli system	0.4	3.5	1.4	0.3	0.2	0.2	6.0
Measurement system	0.4	4.1	1.6	0.4	0.3	0.2	7.0
Power system		2.0					2.0
Control system							
Environmental control system		2.0					2.0
Data processors		50.0					50.0
Switching networks	0.6	7.8	3.3	0.6	0.4	0.3	13.0
Special panels/ displays	0.1	1.2	0.4	0.2	0.1		2.0
Cables/harnesses	1.4	2.8	1.6	0.6	0.3	0.3	7.0
Enclosures/racks	0.5	5.7	2.5	0.6	0.2	0.5	10.0
Software							
Executive						1.0	1.0
Unit under test							
Documentation							
						2.5	100.0

TABLE III

Test Equipment Cost Element
SCTS

Cost Element Subsystem	Material	Parts	Fabri-cation	Assembly	Inspection	Support	Percent Production Cost
Hardware							
Stimuli system	0.6	5.8	2.4	0.5	0.4	0.3	10.0
Measurement system	0.7	7.1	2.8	0.6	0.5	0.3	12.0
Power system		4.0					4.0
Control system							
Environmental control system		2.0					2.0
Data processors		25.0					25.0
Switching networks	1.0	12.0	4.4	1.2	1.0	0.4	20.0
Special panels/ displays	0.1	1.2	0.4	0.2	0.1		2.0
Cables/harnesses	2.6	5.2	3.0	1.2	0.5	0.5	13.0
Enclosures/racks	0.1	7.0	1.8	0.3	0.3	0.5	10.0
Software							
Executive						0.5	0.5
Unit under test						1.5	1.5
Documentation							
						4.0	100.0

TABLE IV

Test Equipment Cost Elements
CP713

Cost Element Subsystem	Material	Parts	Fabri- cation	Assembly	Inspection	Support	Percent Production Cost
Hardware							
Stimuli system	2.4	23.2	8.4	2.8	2.4	0.8	40.0
Measurement system	0.6	12.6	3.8	1.4	1.2	0.4	20.0
Power system		6.0					6.0
Control system							
Environmental control system							
Data processors							
Switching networks	0.4	5.4	2.2	0.6	0.3	0.1	9.0
Special panels/ displays	0.5	2.9	1.0	0.3	0.3		5.0
Cables/harnesses	2.6	5.3	3.0	1.1	0.5	0.5	13.0
Enclosures/racks		6.6		0.3		0.1	7.0
	6.5	62.0	18.4	6.5	4.7	1.9	100.0
Software							
Executive							
Unit under test							
Documentation							

TABLE V

Cost Drivers

System Requirements	Engineering/ Documentation	Procurement	Eng Tests	Fab and Proc	Assembly	Fact Test and Insp	Support (Prod Control)	Life Cycle
MIL Environment	Form 1 Documentation	Tolerance Specs	Multiplicity of unique test sets	New unfamiliar processes	"Star" value components	Multiplicity of unique test sets	Quantity of items to be manufactured	Personnel
Equip class		Non-Standard Parts						Vehicles frequency and complexity of maintenance cycles
Nuclear/EMI				Solder connectors		Inadequate test points		
Reliability				Shielded wire		Realistic tolerance tree		Multiplicity of unique test sets
Tolerances								
Speed								Non-standard parts
Autonomy	Software batch compiler	Computer		Multilayer boards		Manual test equip		

System Requirements

Specification of unnecessarily tight tolerances whether they be mechanical or measurement is costly. The cost in manhours to machine to ±0.001 versus 0.005 is approximately 3 to 1. A 0.1 percent measurement will increase testing cost by a factor of five over a 0.5 percent measurement.

Speed of testing may drive test equipment costs both in software and hardware. Real-time testing may drive software to a lower level language.

Form 1 engineering documentation requires approximately 30 percent more effort than use of good commercial practices. For test and training equipment, strong consideration should be given to eliminating requirements for form 1 documentation, particularly where small quantities are involved.

Non-standard parts are expensive to a system. Not only do they often cost more, because quantities required do not reach price break levels, but they also impact life cycle costs because they generate another line item in the inventory.

A large system such as Pershing has many separate and distinct test sets because of the many and various types of tests which must be performed. Universal test systems have generally proven unsuccessful because of the large costs involved. An alternate approach to a solution of the problem would be universal "smart" modules.

New and unfamiliar processes should be avoided in the design of equipment where small quantities are involved and learning curves therefore cannot be applied.

Solder connectors require approximately twice the time required for crimp connectors.

Shielded wire, besides being somewhat less reliable, requires about twice the time of a single connector.

Star-valued components have a double cost impact. The selection, installation and test takes about 30 minutes longer than a non star-valued item. Because of stocking requirements the procurement costs are about 10 times higher.

Adequate test points are a must for economical factory testing. For every needed test point not provided the time to test that function increases by a factor of ten.

A realistic tolerance tree should not use worst case. Tolerances should be statistically averaged to optimize factory yield versus time. This could possibly be the subject of a study to generate proper methods of establishing tolerance trees. These trees should start at the lowest specification level (component) and be carried up to the user location. All lower level specifications must be tailored to a probability that the next level specification can be met.

For the most part, life cycle costs are determined by the number of personnel required to operate and support (O&S) the system. Manufacturing Technology proposals 1 and 2 are aimed at reduction of these costs. For the Pershing system the yearly O&S costs are approximately 0.8 times the cost of the original equipment (less the missile round). This means that for 10 years the O&S costs are eight times the original acquisition costs. It is interesting to note that on Pershing, personnel and battalion support increased 5 percent in 1973 over 1972 and 16 percent in 1974 over 1973.

Pershing and SPRINT I offer a meaningful comparison of on-line versus batch compiling of test programs. Pershing programs must be assembled or compiled on a large data-center computer whereas the SPRINT I programs can be assembled or compiled on-line. Pershing program changes or corrections require a minimum turn around of 24 hours with a typical time of 3 days. This problem is further compounded for classified programs since housekeeping requirements have forced the data center into a posture of accepting classified work only twice a week. Although the most important factor is schedule delays, the machine time charge by the data center is not insignificant. SPRINT I program assembly or compilation is completed under the programmer's control. Small changes in the program can be accomplished in a few minutes. Program quality is improved because the programmer can compare alternate approaches for optimization. Based on Pershing/SPRINT experience a rule-of-thumb is proposed: If the data center bill for two years exceeds the cost of installing test program online development capability, substantial dollar savings can be realized by going online.

Manual test equipment in the factory significantly increases test costs. Reductions of 85 to 90 percent can be realized by using fully automated testing rather than manual testing.

MANUFACTURING TECHNOLOGY PROJECTS

Title: Manufacturing Technology Project to Provide Specifications and Costs for Standard "Smart" Test Equipment Modules.

System/panel area/component: Pershing/Test and Checkout/Test Equipment

Problem

Large systems generally breed a large number of different special test sets with the attendant O and M costs. Universal test sets because of their complexity have not proven to be the panacea for this problem. The modular approach would allow a test set of the required complexity to be put together.

Proposed Solution

Perform a study of many systems to establish the parameters which must be measured, their tolerances, timing requirements, etc. Then write specifications for modules which use microprocessors for "brains." Several much modules could satisfy the majority of the requirements for electronic testing.

Project Cost and Duration

Benefits

Reduction in engineering and factory test costs and reduction in O and M costs.

Title: Manufacturing Technology Project to Provide an Automated Means for the Removal of Compound Coating for Printed Circuit Board Fault Isolation

System/Panel Area/Component: Pershing/Test and Checkout/Printed Circuit Boards

Problem

Printed circuit boards are a large cost item. No good way exists to remove conformal coating so that fault isolation of printed circuit boards can be automatically performed. This increases both factory rework and O and M costs.

Proposed Solution

Perform a study of this problem with the following as suggested candidates:

1. Look into different coating means in an attempt to find one with acceptable qualities which could be chemically removed.

2. Look into chemicals which could remove presently approved coatings without board or component damage.

3. Study mechanical means such as sandblasters, lasers, or hot-spatula, numerically-controlled devices.

Implement the most likely solution.

Project Cost and Duration

Benefits

Reduction in factory rework and O and M costs.

ACKNOWLEDGEMENTS

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CHAPARRAL TEST EQUIPMENT

B. B. Pegg

Aeronutronic Ford Corporation

Aeronutronic Division

Newport Beach, California 92663

CHAPARRAL MISSILE SYSTEM DESCRIPTION

The Chaparral Guided Missile System, (Figure 1) one of the Army's very effective and successful missile systems, is a highly mobile system currently fielded to provide world wide protection to the forward area of the field Army against hostile aircraft flying at low altitudes. Variations of the Chaparral system make it suitable for fixed emplacement. Shipboard adaptations (Figure 2) have been demonstrated and have provided the Navy with an anti-ship missile defense capability. The missile used by the Chaparral System is a ground-to-air adaptation of the Sidewinder Air-To-Air heat seeking missile.

FIGURE 1

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FIGURE 2

The basic configuration of the Chaparral Missile System is the M48 Fire Unit. The M48 Fire Unit is highly mobile and comprises the M54 Launching Station mounted on an M730 Tracked Vehicle. This M730 tracked vehicle is an M548 Cargo carrier with minor modifications. Figure 3 shows the major system components. The M54 Launching Station has provisions for twelve MIM-72 missiles, four on the launch rails and eight stored in integral stowage compartments. The missiles may be one of three versions:

(a) MIM-72A Chaparral Missile.

(b) MIM-72B Chaparral Training Missile.

(c) MIM-72C Improved Chaparral Missile.

WEAPONS SYSTEM TEST EQUIPMENT (WSTE)

General

This presentation describes the test equipment associated with the Chaparral System. Since most of the equipment associated with this program was developed approximately ten years ago, no attempt will be made to show a detailed cost analysis. Instead a general description of the various test equipments utilized will be presented. One exception will be made, where relative costs on a current basis are available, this exception being the launcher test set (AN/TSM-85). This test set has been produced in a total quantity exceeding 100 units and is currently being procured in small quantities.

Test Equipment for Chaparral can be divided into two major categories, namely Field Test Equipment commonly referred to as Weapons System Test Equipment (WSTE) and Production Support Equipment comprised mostly of by Special Acceptance Inspection Equipment (SAIE). Each of these major categories have two subcategories, namely the missile test equipment and the launching station test equipment.

WSTE Description

Table I shows the breakdown of fielded test equipment used to support the M54 Launching Station.

Table II lists the Missile Field Test Equipment used to support the MIM-72A Missile and MIM-72B adaptation. This missile is in the current inventory associated with Chaparral.

The items classified as Weapons System Test Equipment, as previously mentioned, were developed approximately ten years ago. Several pieces, such as the M-71 launcher aligment fixture and the AN/DSM-79 Missile Tester are adaptations of items previously used on other military programs.

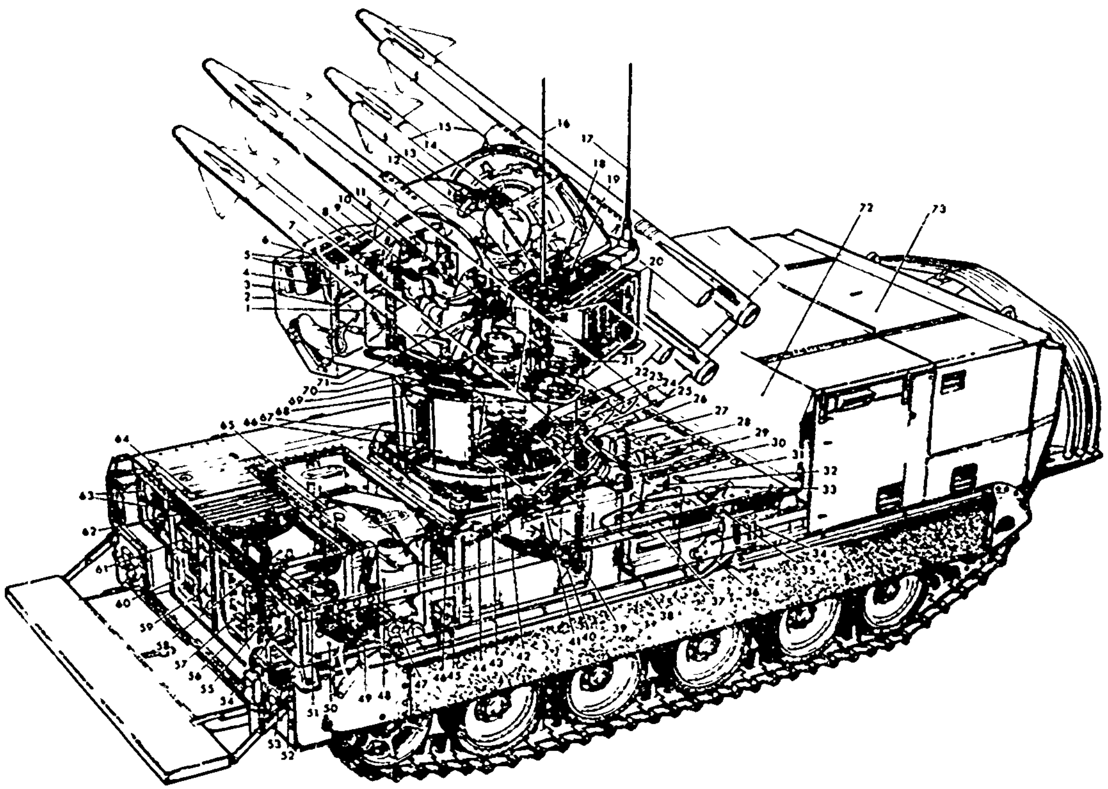


FIGURE 3

TABLE I. WEAPONS SYSTEM TEST EQUIPMENT CHAPARRAL LAUNCHING STATION (M54)

Name	Designation	Description and Use
Test Set, Guided Missile System	AN/TSM-85	This is a portable tester used to perform fault isolation tests in the field on the M-54 Launching Station. It is housed in two metal cases. One contains the Test Set Assembly and the other the Cable Assembly Group. The test set assembly contains: a meter circuit for measuring voltages and resistances on a 0 to 10 scale, external meter jacks, test switches allowing connection of the test set to various signals in the fire unit and routing test signals from the test set to the fire unit.
Alignment Set, Launcher	M71	This is a portable optical sighting fixture in a metal case. Three pieces, joined, allow check and adjustment of alignment between gunner's sight and the launch rails. The assembled alignment set incorporates two hangers, similar to those on the missile, for installation on the launch rails. The center section contains an elbow telescope.
Shop Equipment, Guided Missile System (Support Maintenance Shop Set)	AN/TSM-96	This heli-hut shop set provides facilities and test equipment for test and fault isolation of fire unit components to a support maintenance level of replacement. By use of the AN/TSM-101 Test Set, faults are isolated to a circuit board or other replaceable assembly. It is also used to test the TSM-85 and the DSM-79 test sets. The shop set is truck transportable, environmentally controlled, and uses a trailerized 25 kW, 208 V, 400 Hz Power Supply.
Test Set, Guided Missile System	AN/TSM-101	This test set, the principal item in the AN/TSM-96, is a shock-mounted, three-bay console with electronic equipment for fault isolation and repair of units under test. It contains standard test equipment, two control-indicator panels, power supplies, two connector panels and a power distribution panel. A cable group is used for connection of each unit under test to the test set.

TABLE II. WEAPONS SYSTEM TEST EQUIPMENT CHAPARRAL MISSILE (MIM-72A AND MIM-72B)

Name	Designation	Description and Use
Shop Equipment, Guided Missile System (Organizational Maintenance Shop Set)	AN/TSM-95	This heli-hut shop set provides work and storage space for equipment used in isolating system faults to an organizational replacement level. It also provides for assembly and disassembly of missiles, as well as the capability for test of missile guidance sections. The shop set is truck transportable, environmentally controlled and uses a 25 kW, 208 V, 400 Hz trailerized power supply.
Test Set, Guided Missile	AN/DSM-79	The AN/DSM-79 is used to test the guidance section of the missile. It is a self-contained unit in a two-piece aluminum case. It consists of an electronic section, a mechanical section, and a group of accessories stored in the cover half. This tester is used in conjunction with the pneumatic subsystem in the AN/TSM-95 shop set, and the available 400 Hz, 115 V power supply. This test set is automatically programmed, and performs ten dynamic tests on the guidance section, with a GO-NO-GO readout in 2-1/2 minutes.

Design/Cost Drivers for Launcher WSTE

The shop sets and the Launcher Test Set (AN/TSM-85) were designed concurrently with the design of the Chaparral M54 Launching Station. While cost considerations were definitely a factor, primary goals for designing these equipments were (1) effectiveness in trouble isolation, (2) portability, (3) ease of operation, (4) world wide usage, and (5) ease of maintenance of the testers themselves. Large scale production was not attained on any of the items. The AN/TSM-85 was produced in a total quantity in excess of 120 units during several procurements. This unit is currently being produced in small quantities and Figure 4 shows the current relationship of materials versus labor for its major components. The percentages depicted are based on these very small quantities and would no doubt be different if a large scale production run was made. In any event, the quantities involved are such that cost reductions in this area have minimal total program cost impact and, therefore, is not a fertile ground for cost reduction programs.

Cost Reduction Already Accomplished on Missile WSTE

So far in this discussion, the descriptive material presented for support of the missile in the field (Table II) has been based on the MIM-72A and MIM-72B versions of the Chaparral Missile. The Improved Chaparral Missile, MIM-72C utilizes a redesigned guidance section, AN/DAW-1. During the recent improvement program which resulted in a significant improvement in missile performance and reliability, attention also was directed to minimize the field support required. This was achieved. The test equipment required to support the MIM-72C guidance section will be an IR flashlight. This will permit the guidance section to be handled as a "round". If it meets the IR flashlight test, it is suitable for flight. This approach will permit the phasing out of the AN/DSM-79 Missile Test Set and eliminate the requirement for an air compressor system

FIGURE 4. AN/TSM-85 CHAPARRAL GUIDED MISSILE LAUNCHER TEST SET COST ALLOCATION BY MAJOR ITEM

TEST SET

CABLE SET (30% OF TOTAL)	LABOR	MATERIAL	TEST CONTROL UNIT (70% OF TOTAL)	LABOR	MATERIAL
CASE*	2%	98%	CASE*	2%	98%
CABLES*	4%	96%	CONTROL PANEL	35%	65%
			CARDS	33%	67%
			HARNESS	96%	4%
			MISCELLANEOUS	60%	40%

*PURCHASED ITEMS

within the AN/TSM-95 Organizational Maintenance Shop Set. This shop set will probably be retained as a missile assembly shelter.

Summary

We believe the Chaparral launcher WSTE has been a cost effective design and, therefore, is not a useful area for cost reduction efforts. This was accomplished largely by simplicity of design approach and concurrent design of test provisions into the production, rather than the all-too-common approach of designing the test equipment after the product is designed. In the design of the Improved Chaparral Missile the user overall cost problem (hardware and personnel) was recognized and worked by designing the product to substantially eliminate the need for missile WSTE.

FACTORY SUPPORT EQUIPMENT

General

So far we have considered the test equipment fielded as part of the Chaparral System. The test equipment used in the production of a system can have a marked influence in the cost of a product. As with the fielded test equipment, let us separate the M54 Launching Station production equipment from the missile equipment.

M54 Launching Station Production Test Equipment

Factory test equipment used to support the production of Chaparral launching stations is primarily in the Special Acceptance Inspection Equipment (SAIE) category. This equipment was designed, documented and controlled to provide points of acceptance by the customer, in this case, the Missile Command of the Army. Key characteristics that related to points of acceptance included:

(a) Specified Performance Parameters.

(b) Quality Requirements.

(c) Spares Requirements.

In addition, other factors influenced the design of this test equipment such as quantities ultimately to be produced, production rates, and last but by no means unimportant - how much will it cost, are major factors.

Design of the SAIE for Chaparral occurred concurrently with the product development. This permitted testing considerations to be incorporated into production configuration. This fact probably contributed greatly to the relative simplicity of the Chaparral Test Equipment. Launching Station production rates were approximately 20 per month during parts of the initial production period of 1967 to 1971. The total quantity of M54 launching stations produced was in excess of 400 units. By careful standardization and maximizing usage of available commercial equipment such as oscilloscopes, digital voltmeters, power supplies, stimuli generators, counters, etc., equipment costs were kept to a minimum. This also resulted in long term low costs for calibrations and maintenance.

Table III shows the SAIE utilized during the M54 launching station production. Also indicated are the SAIE that was duplicated for use at the Chaparral Depot located at Red River Army Depot. Since the depot was tasked to maintain, repair and return to the field, equipment that is equivalent to a newly produced item, the decision to duplicate the factory SAIE permitted "like factory" testing and also resulted in a lower cost because no design effort was expended to satisfy depot needs. To supplement the SAIE in fault isolation and troubleshooting, additional test fixtures were also supplied. These supplemental test fixtures, referred to as Fault Isolation Test Fixtures, FITF, have since formed the nucleus for small quantity user depots.

Several representative pieces of Chaparral SAIE are illustrated in Figures 5 through 8.

Even though designed and fabricated almost ten years ago, this SAIE was used until 1971. In 1973, this equipment was returned to active use to support additional building of Chaparral launching stations, with a very minimal amount of refurbishment.

Again, no specific cost drivers have been identified as being pertinent to cost reduction efforts since design for long term usage has resulted in a very cost effective set of SAIE.

Missile Guidance Section Production Test Equipment

Background. The Chaparral MIM-72A and MIM-72B missiles have been produced in significant quantities. The Chaparral missile production when added to the overall Sidewinder missile production, results in a very large total quantity. Since all of the Chaparral MIM-72A and MIM-72B missiles were produced by manufacturers other than Aeronutronic Division of Aeronutronic Ford Corporation, no attempt will be made to describe the variety of SAIE that has been used or still exists. The Aeronutronic Division is currently proposing to MICOM the initial production of the improved Chaparral Missile MIM-72C. This production program for the MIM-72C missile will utilize approximately twenty pieces of SAIE to support this procurement. As a cost savings approach, it is planned to use many pieces of equipment from other missile buys, this equipment having been supplied to Aeronutronic as government furnished property. In addition, a number of stations will be designed and fabricated to test the improved performance requirements of the AN/DAW-1 guidance section. These manually operated or semiautomatic type of testers in most cases will cost effectively meet typical production rates.

TABLE III. CHAPARRAL M54 LAUNCHING STATION SAIE

Tester	Purpose	Also Used at Depot
Chaparral Control Units Tester	The control units tester performs checkout and acceptance tests on eight different Chaparral missile control unit assemblies and the voltage regulator prior to their use or installation.	Yes
Circuit Board Tester	The circuit board tester assembly is used to checkout and acceptance test selected circuit board assemblies from the Chaparral fire unit, units test set, and the launch and control test set. There are 52 configurations of circuit boards tested by the Circuit Board Tester Assembly.	Yes
Power Supply Tester	The Chaparral power supply assembly and module tester performs checkout and acceptance tests on the power supply each of the three power supply modules; and four submodules.	Yes
Mount Drive Control Box Tester	The mount drive control box tester performs checkout and acceptance tests on the mount drive control box as a complete assembly prior to its installation or use in the guided missile system.	Yes
Power and Pneumatic Subsystem Tester	The power and pneumatic subsystem tester performs checkout and acceptance tests on the completed launcher base.	Yes
Launching Station System Tester	The launching station system tester provides a means of performing checkout and acceptance tests of the guided missile system with all assemblies installed.	Yes

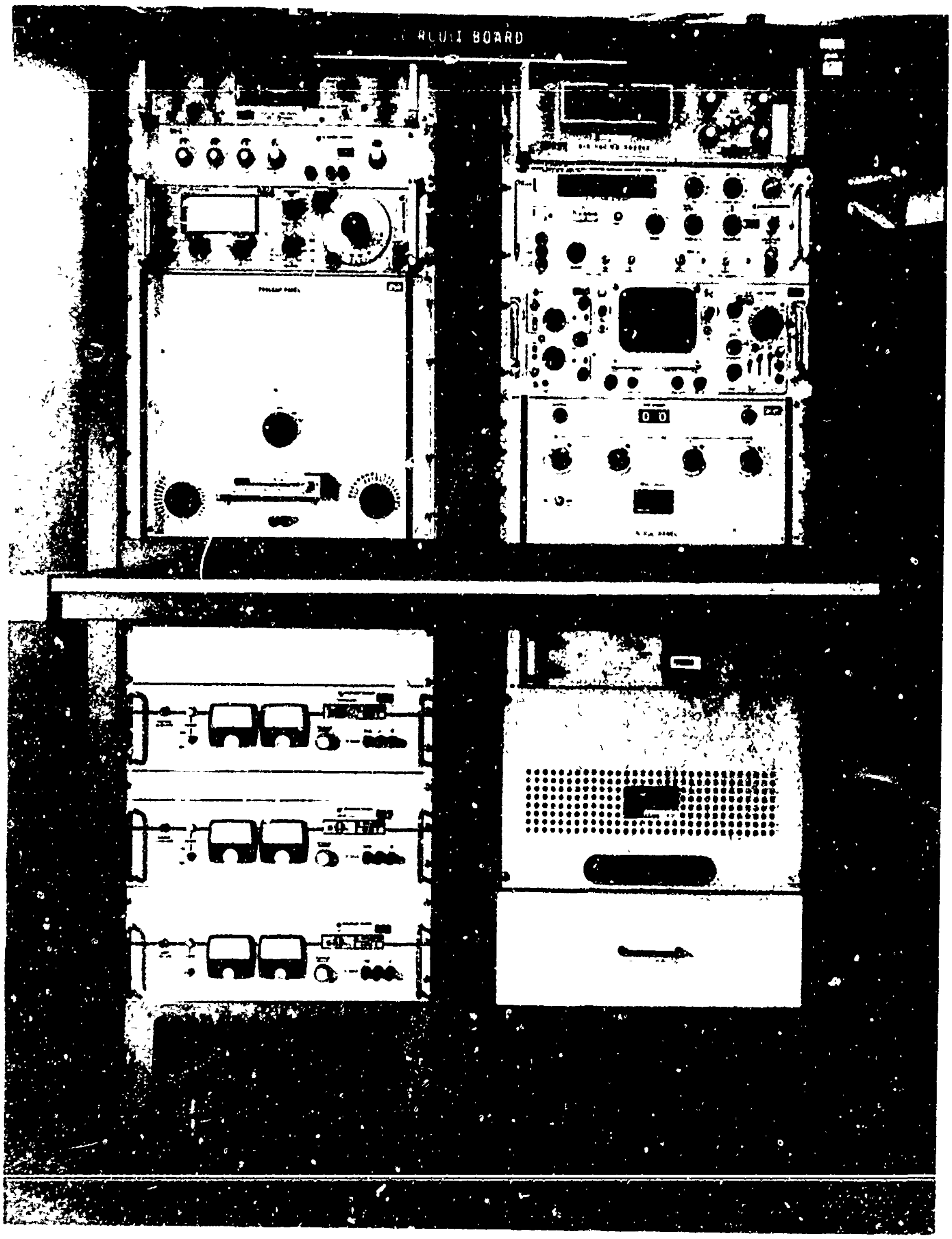


FIGURE 5

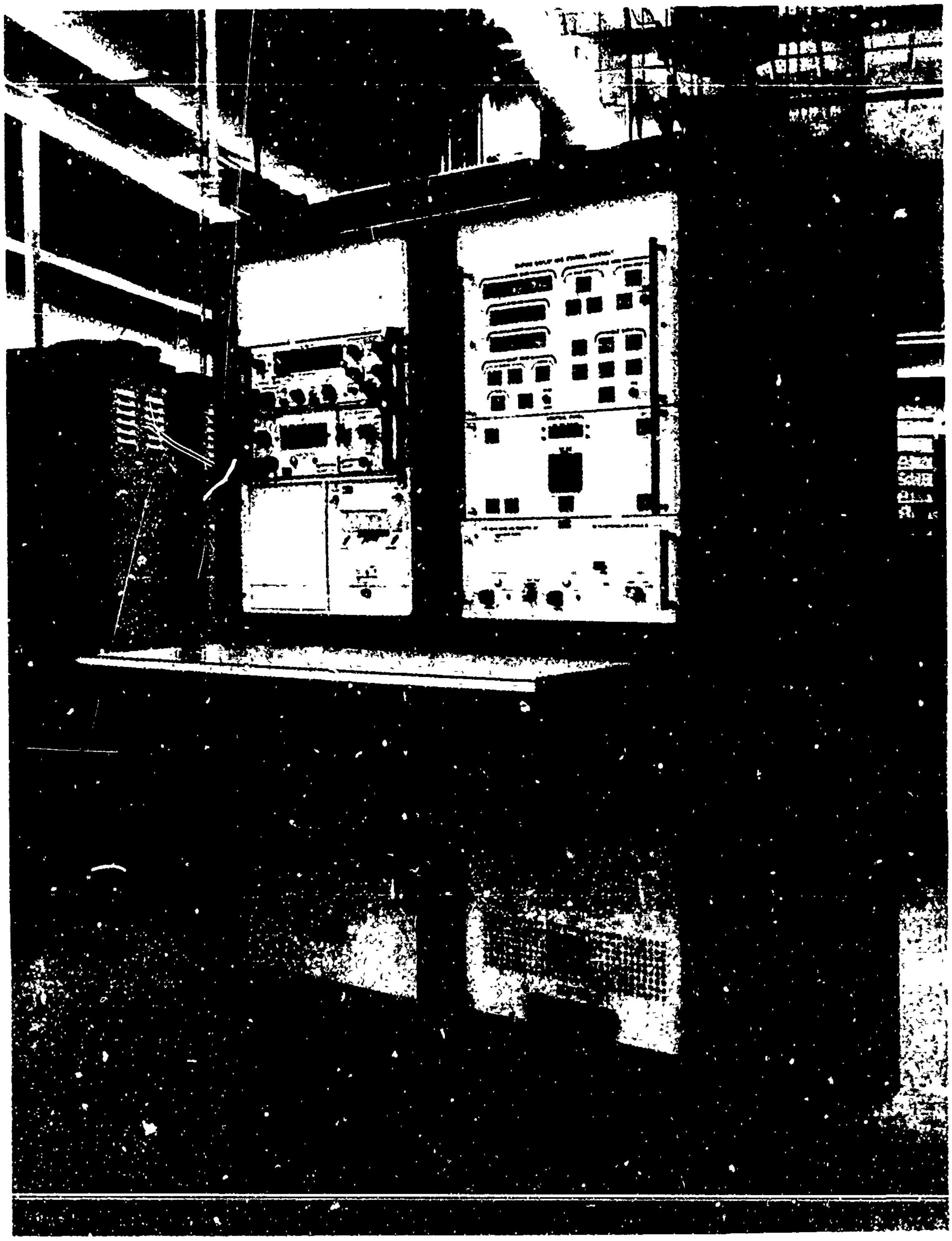


FIGURE 6

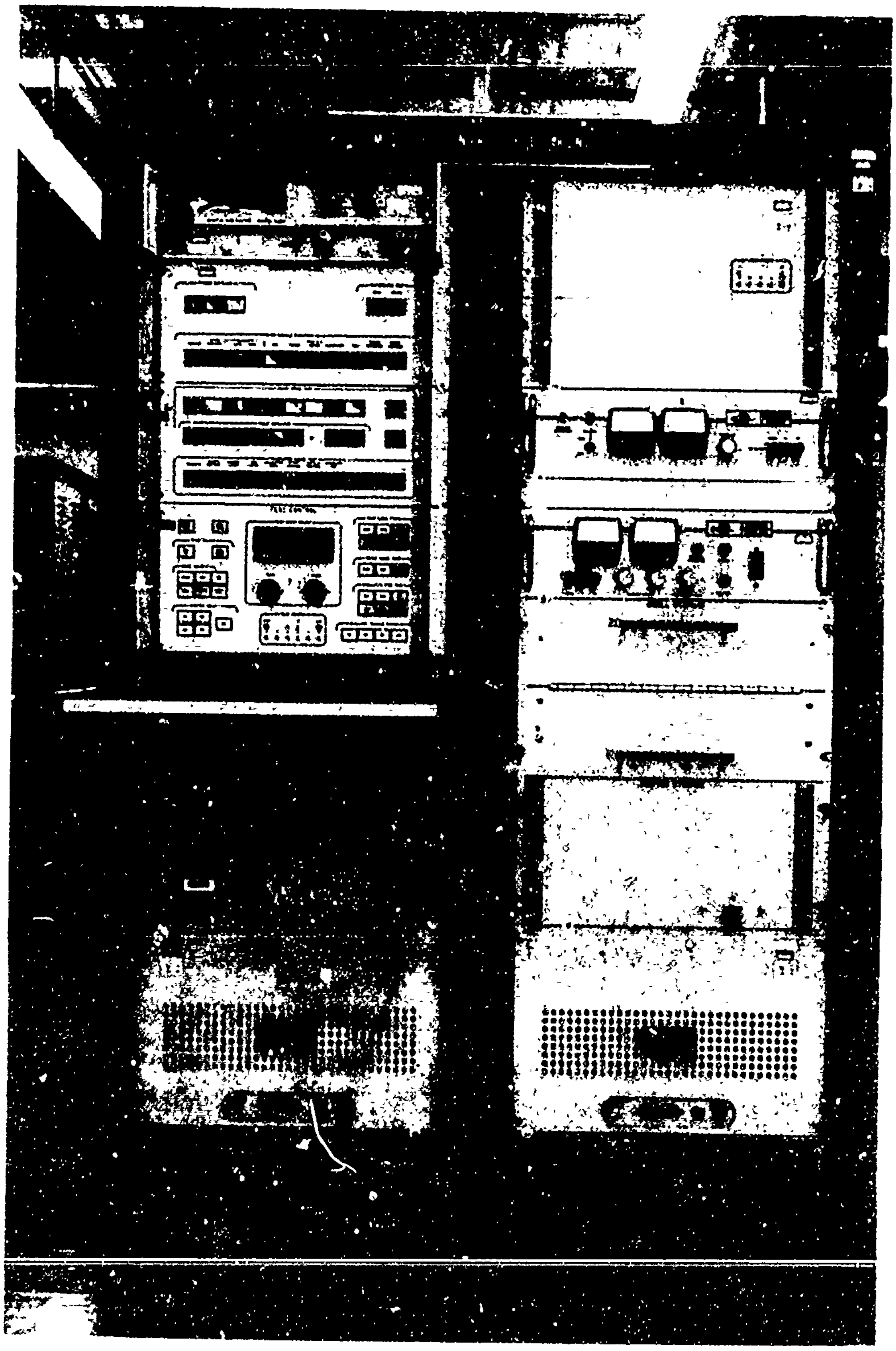


FIGURE 7

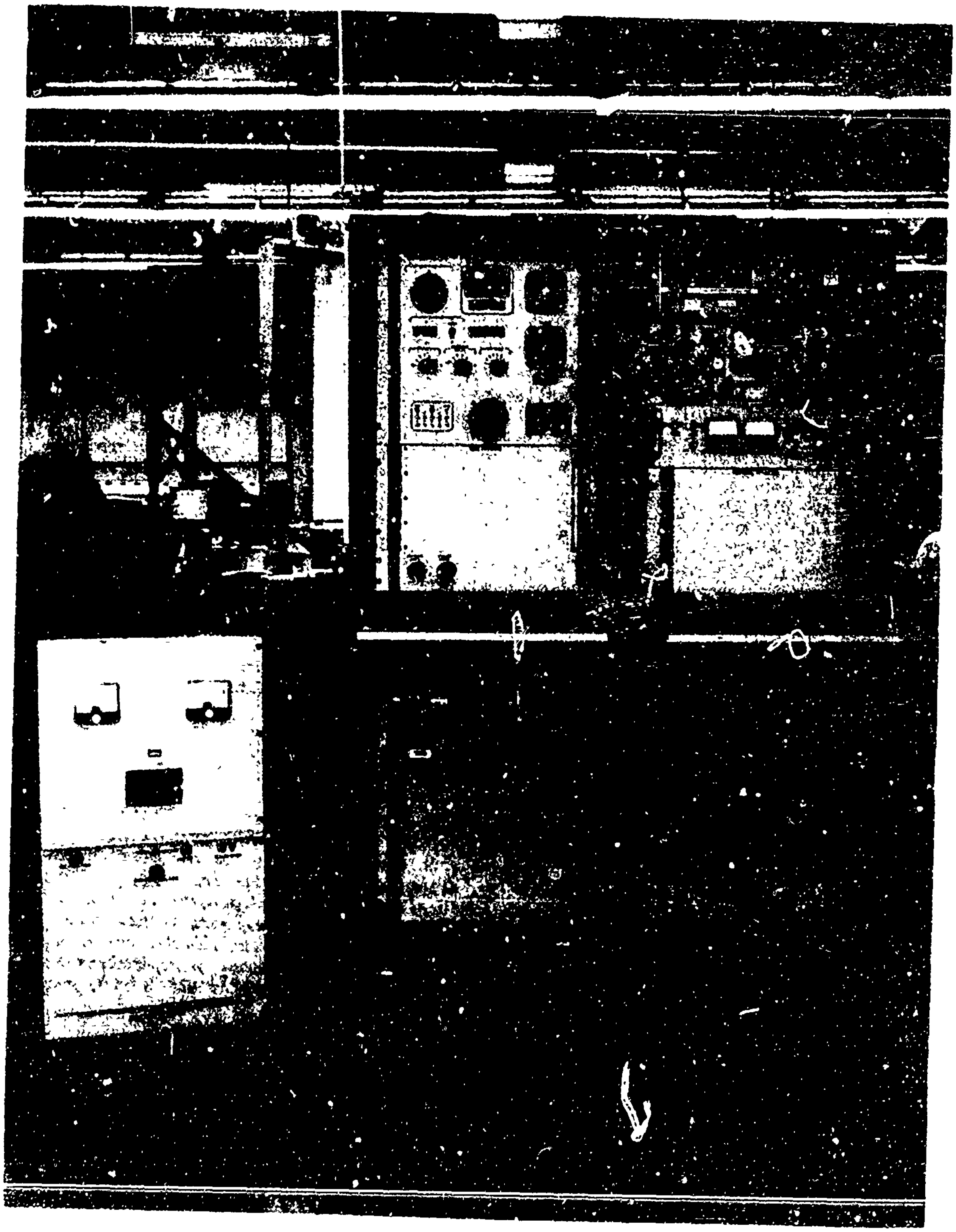


FIGURE 8

Cost Improvement Area. No attempt will be made to identify a project associated with test equipment that would lead an effective lowering of missile systems costs. The technology required to create test equipment that would result in long term cost reductions already exists. Computer control, micro processors, and similar technology are available today and would permit building test equipment that would greatly reduce operator test times. This reduction in operator test time is a significant step in reducing overall missile systems costs. The problem is -- how can these improved technologies be utilized effectively? This may not require a project however it could appear to take on the status of a major program. Test equipment, especially that used in support of a production program, is usually procured as part of an initial production effort. This initial production procurement, because of funding policies, usually must stand alone. Its costs must be justified and be within the funds available for the current fiscal year. As additional procurements are planned for future needs, each procurement must stand alone. This is necessitated because of funding policies, and the desire to keep each procurement open for competitive bidding. This is where test equipment and the testing operation costs start to show up in this cost cycle. Since most single buys are for a limited quantity and a missile producer can only gear up for this single limited quantity, he uses less than optimum efficiency in the designing of test equipment and as a result has higher-per-unit cost associated with each missile produced. This results in higher costs on the initial buy. Because of competitive follow-on procurements, not only does the initial manufacturer again quote using the nonoptimized techniques, but his competitors must also follow suit. As a result long term missile systems costs stay high and never have the opportunity to take advantage of large volume, long term planning. The solution is to somehow separate the test equipment costing during initial procurements and have it priced out based on a realistic long term production program, even if the long term procurement must occur over several fiscal periods. This would also permit the initial procurement to have the advantages of this optimized test equipment. Since this test equipment would be government owned equipment, competitive follow-on procurements could be based on the successful bidder using this government owned equipment.

The challenge to the government is to overcome all of the obstacles in currently planning methods and take advantage of long term planning and its ultimate reduction in systems costs, schedules permitting.

CONCLUSIONS AND RECOMMENDATIONS

Chaparral test equipment experience demonstrates the importance of establishing the testing approach as the product is being designed, and influencing the product design accordingly, so that the product is "testable" with a minimum burden on the test equipment design. If this principle is adhered to, along with a "keep-it-simple" philosophy, the cost of test equipment to support items produced in relatively low quantity should not be a significant program cost variable. Further, this approach tends to make the test equipment good the first time and suitable for long term use and reduces the need or desire to make "improved" new versions. A companion consideration, being implemented with the Improved Chaparral Missile, is to design the product so that field test is not required, or at least is minimized.

In the area of missile production test equipment it is recommended that this test equipment be planned and built during the initial production phase taking into account optimum future production rates, and most importantly, base the test equipment upon the total expected production in the years to come, even though approval i · that future production has not been obtained.

FACTORY TEST EQUIPMENT MICRO-PROCESSOR AND AUTOMATIC FAULT ISOLATION APPLICATIONS

J. L. Farnsworth

Hughes Aircraft Company

Tucson, Arizona 85734

INTRODUCTION

The Tucson Manufacturing Division of the Hughes Aircraft Company is currently involved in the manufacture of Missile Weapon Systems for the Army, Navy, and Air Force Departments. In addition to the ongoing high rate production of the Army TOW Missile, this Division is now implementing for production of the U.S.-ROLAND Missile and participating in the development of the HELLFIRE Missile which, if the Hughes Aircraft Company is the successful contractor, will also be produced at the Tucson, Arizona, facility under contract with the U. S. Army Materiel Command.

For the past 23 years The Tucson Manufacturing Division has been active in the high rate production of missile systems of medium to high complexity. In support of these missile programs, this Division has developed and implemented a variety of automatic and manually operated test and inspection equipment. The three major ongoing missile production programs are currently utilizing 277 test stations; of which 26 are operated under computer control and another 51 are of the punched card, tape or hardwired controller variety. Automated equipment represents 28% of the test equipment complement at the Tucson production facility and the benefits derived from this automation have proven to be extremely cost effective. This information is presented in Figure 1, Tucson Manufacturing Division Test Station Complement.

TUCSON MANUFACTURING DIVISION TEST STATION COMPLEMENT

TEST STATION CATEGORY	NUMBER OF TEST STATIONS	%
Automatic - Computer Controlled	26	10
Automatic - Paper Tape/Punched Card/ Hard Wired	51	18
Manual	200	72
TOTAL	277	100

FIGURE 1

To further illustrate the types of test stations in use at Tucson and those being discussed in this paper, Figures 2, 3 and 4 are photographs of typical test installations. Figure 2 is a manually operated test station used for troubleshooting. This test station was placed in service in May of 1963. Figure 3 is a hardwired automatic test station used for product functional test and was placed in service in August of 1969. Figure 4 is a mini-computer based automatic test station used for product functional test and was placed in service in August of 1972.

GENERAL

It has been our experience over the past years that test technology has progressed along two lines. The accuracy to which measurements can be made and the speed with which they can be made has continuously increased. While the accuracy of a test installation is usually defined by the requirements of the product to be tested, the speed at which this installation will operate is determined by the following manufacturing considerations.

1. Feasibility of automating the test function
2. Cost of implementing a manual system versus an automatic test system compatible with production rate
3. Recurring labor cost associated with using both types of test stations
4. Ease of modification to accommodate changes in the product
5. Floor space requirements
6. Implementation lead times

Based upon these considerations, a decision can be made to automate or not to automate a given test operation.

COST TREND DATA

An analysis has been made of the test effort on the TOW Missile program to identify typical areas in the manufacturing process where meaningful cost reduction techniques have been and can be effected. In performing this analysis, particular emphasis was given to those endeavors which in the past resulted in:

1. Reduction of recurring implementation costs
2. Reduction of non-recurring implementation costs
3. Reduction of recurring manufacturing costs
4. Reduction of manufacturing lead times
5. Improved system performance
6. A responsive, flexible production base

We analyzed only factory test equipment implementation to develop a representative break-out of test equipment implementation cost elements by test station subsystems. This information is presented in Figure 5, Test Equipment Implementation Cost Elements, Factory Test Equipment. The largest single cost element we found in the implementation of new test systems is data processors (controllers, mini-computers, etc.) and the labor effort involved with their use. Since these major implementation cost elements are a by-product of the heavy use made at the Tucson Manufacturing Division of automated test systems to

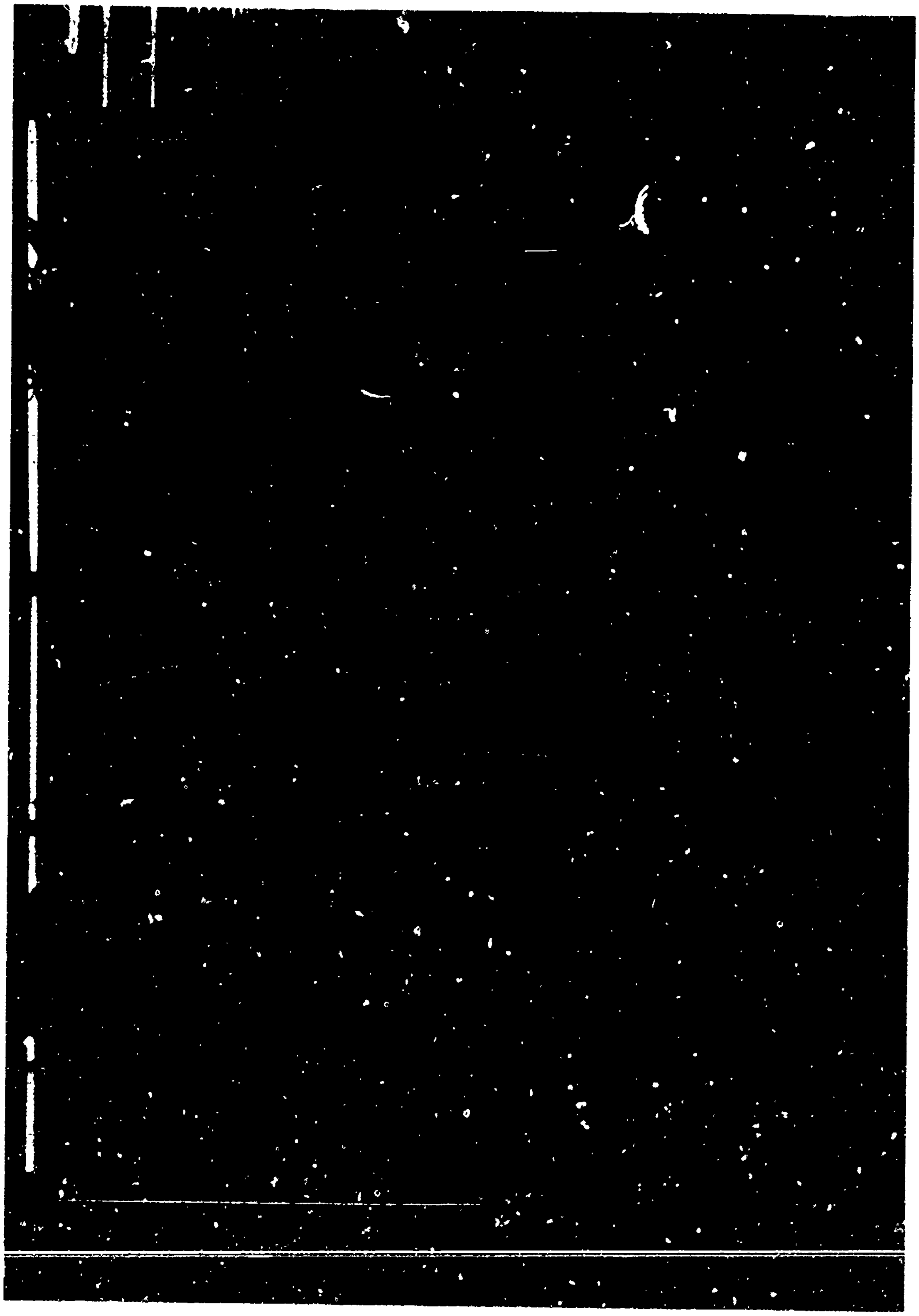


FIGURE 2

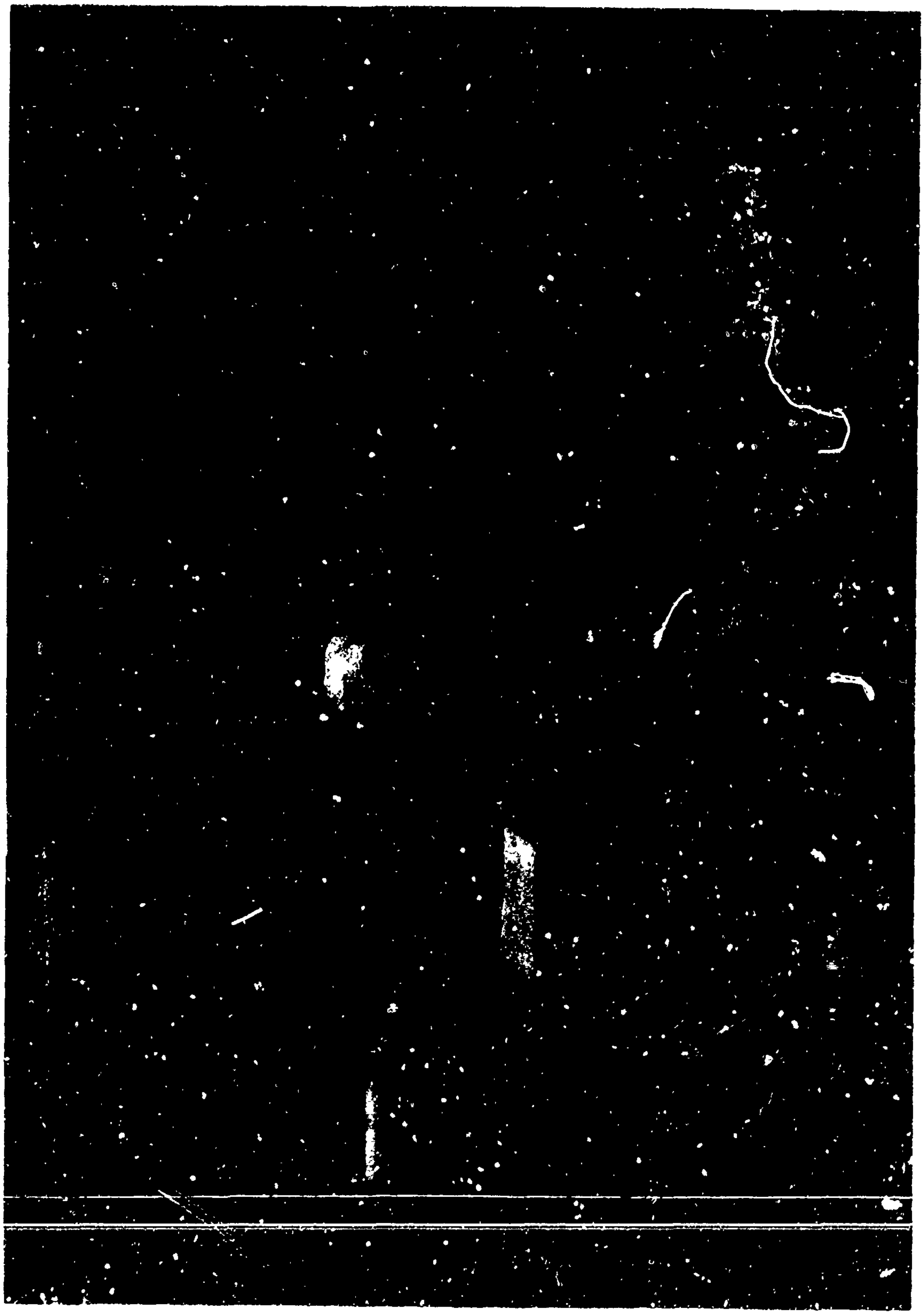


FIGURE 3

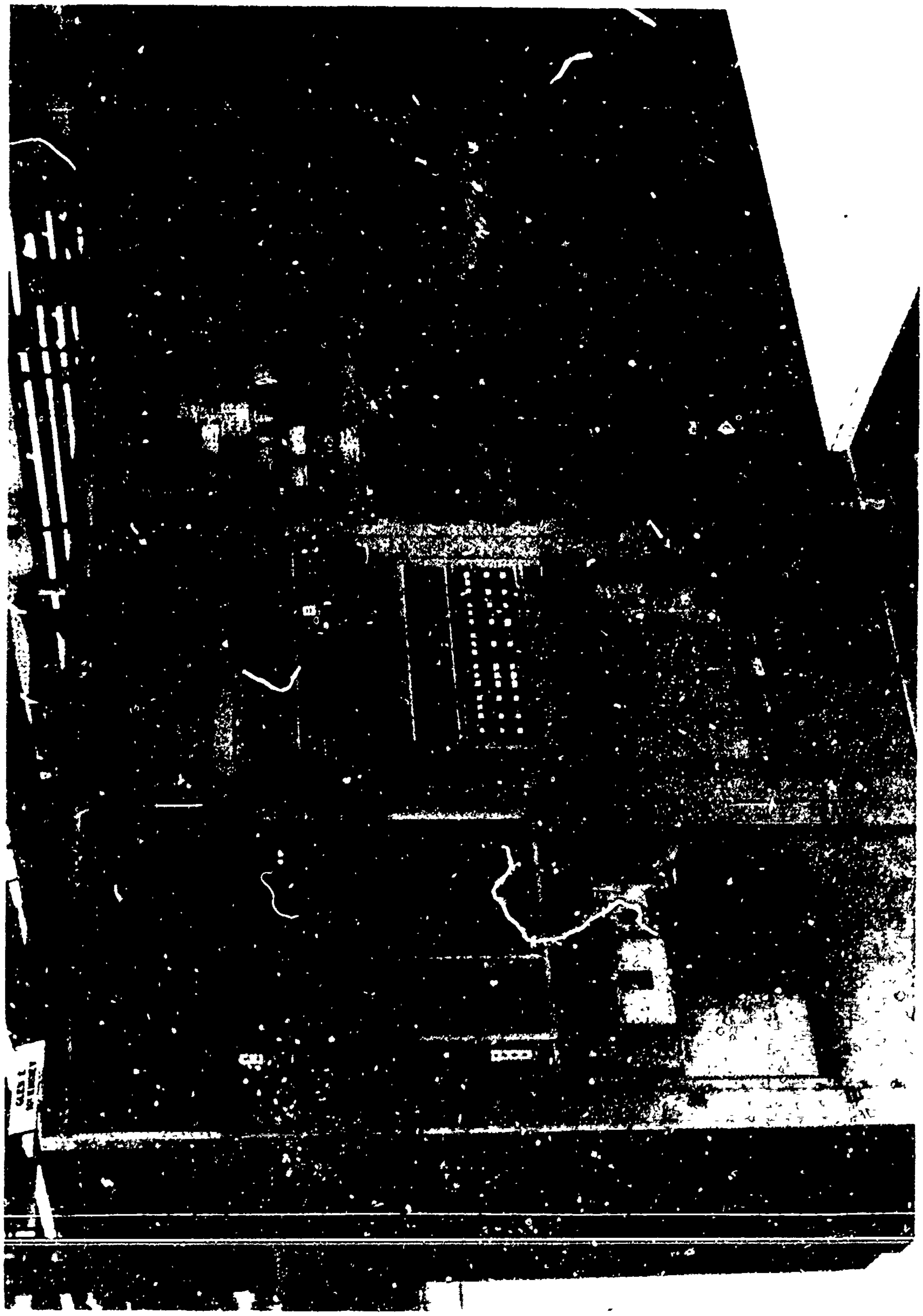


FIGURE 4

TEST EQUIPMENT IMPLEMENTATION COST ELEMENTS

FACTORY TEST EQUIPMENT

(Figure 5)

☐ MAJOR COST DRIVERS

Cost Element / Subsystem	Material	Purchased Parts	Process & Fabrication	Assembly	Test & Inspection	Support	% Production Cost
HARDWARE							
STIMULI SYSTEM	5%	46	6	20	20	3	6
MEASUREMENT SYSTEM	2%	60	3	15	17	3	8
POWER SYSTEM		85	2	3	9	1	1
CONTROL SYSTEM	6%	35	3	40	14	2	3
ENVIR. CONTROL SYSTEM		86		3%	9	2%	1
DATA PROCESSORS		$\boxed{91}$		2	5%	2	25
SWITCHING NETWORKS	5%	30	2	23	18%	5	3
SPECIAL PANELS/DISPLAYS	2%	28	6	40	20	4	4
CABLES/HARNESSES	10	20	7	45	12	6	2
ENCLOSURES/RACKS		96		2		2	1
SOFTWARE							
EXECUTIVE					10	90	11
UNIT UNDER TEST					20	$\boxed{80}$	31
DOCUMENTATION					15	85	4
							100%

MANUAL VERSUS AUTOMATIC TEST CAPABILITIES

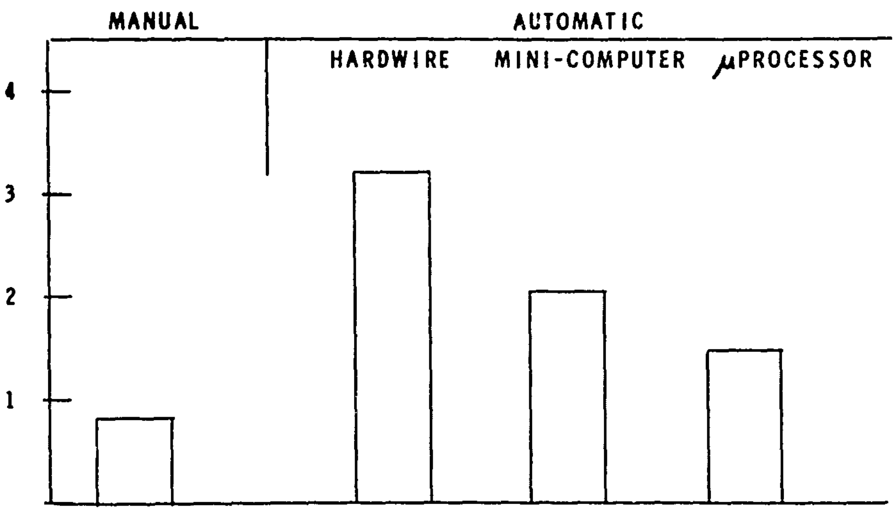
TEST STATION	NO. OF ITEMS TESTED	NO. OF MANUAL TS's REPLACED	MANUAL TEST TIME	NO. OF AUTOMATED T. S.	AUTOMATIC TEST TIME	NO. OF TESTS PERFORMED
MISSILE LEVEL	1	20	16 Hrs.	2	1.5 Hrs.	1,001
SECTION LEVEL	1	7	16 Hrs.	1	1.25 Hrs.	517
UNIT LEVEL	1	7	8.5 Hrs.	1	1.5 Hrs.	841
BOARD LEVEL	6	21	36 Hrs.	1	3.43 Hrs.	864

(Figure 6)

achieve significant reductions in manufacturing test and inspection costs, further investigation was accomplished to quantify the relationships between type of test equipment employed (manual or automatic) and their costs and benefits. As is shown in Figure 6, Manual Versus Automatic Test Capabilities, the use of automated test systems results in not only significant reductions of test time but also in floor space requirements at all levels of assembly since the number of installations required is an order of magnitude smaller.

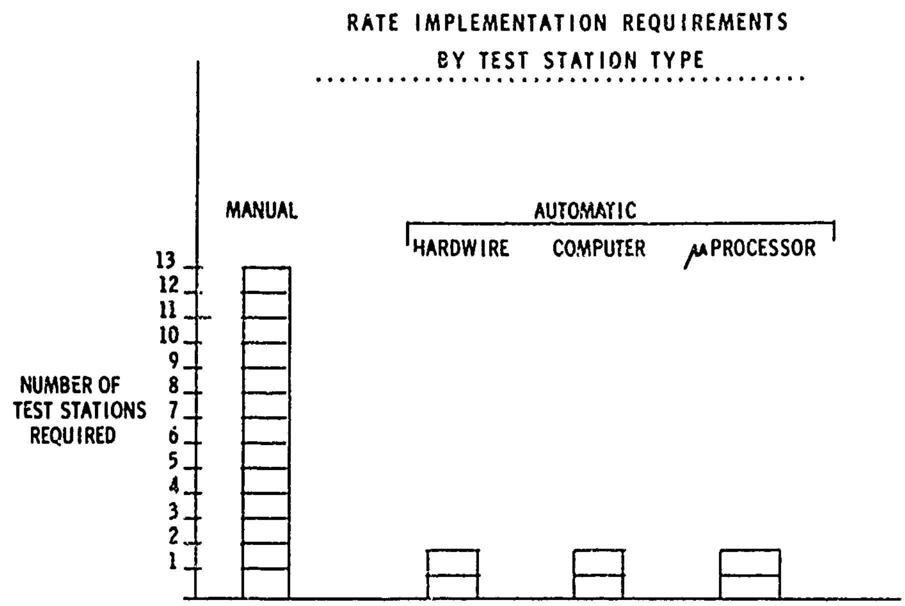
The relative costs of implementing a typical test station for a given item is depicted in Figure 7, Relative Test Equipment Implementation Costs.

RELATIVE TEST EQUIPMENT
IMPLEMENTATION COSTS



(Figure 7)

An automatic station will cost two to three times more to implement than a manual station to perform the same test function. However, due to the relatively slow speed of operation of the manual test station a large number may be required to meet production rate requirements. This typical test station count to meet rate requirements is presented in Figure 8, Rate Implementation Requirements by Test Station Type. For the application depicted, it would require thirteen manual test stations to meet production rate while only two automatic test stations would be required.

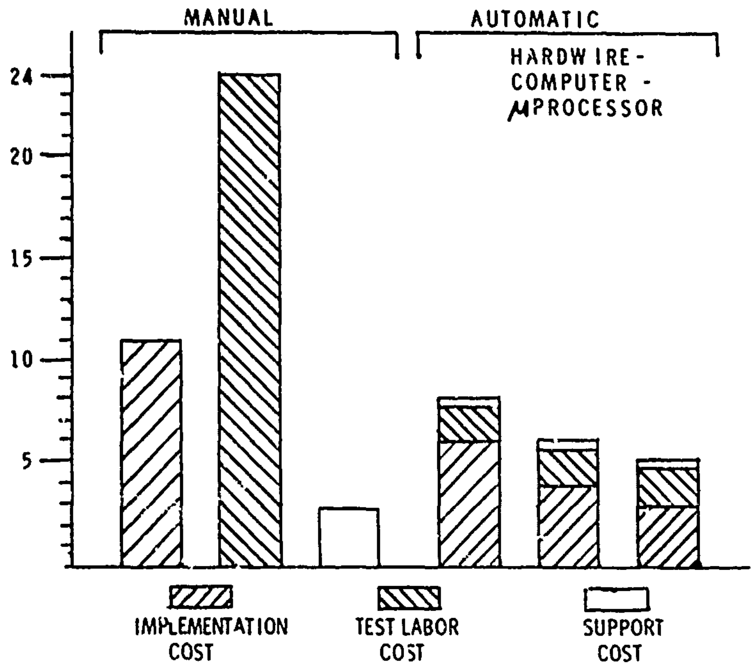


(Figure 8)

In the final analysis, the primary determining factor as to the most cost effective type of test station is the cumulative cost, both recurring and non-recurring, to be incurred over the length of the production run. For this typical test station, Figure 9, Recurring and Non-recurring Cost Comparison, shows the reduction in this cumulative cost which resulted from automation. It is interesting to note that all three bars under the manual equipment heading must be added together to establish proper cost comparison with the automatic equipment bars.

RECURRING & NON-RECURRING COSTS COMPARISON

(100,000 MISSILES)



(Figure 9)

PROPOSALS

In any manufactured product, and certainly, sophisticated missile systems are no exception, recurring labor has to be one of the larger and more universal cost elements. Manufacturing organizations are constantly working to reduce or eliminate labor in their finished product and the most powerful weapon is automation. However, the successful application of automation is currently limited by two obstacles:

1. The high cost of implementing automatic test stations

2. The lack of viable techniques to handle certain classes of test functions which consume high levels of recurring labor

Toward these problems, we propose two manufacturing technology projects.

Micro-processor Based Test System Controller

The first, dealing with micro-processor applications is the development of a low cost test oriented controller which will significantly reduce the cost of new automatic test systems. As was evidenced in the Cost Trend Data the major expenses are associated data processors (test system controllers) and the software they use.

For a number of years we have employed specialized computer controlled and hardwired test equipment to minimize recurring production labor costs. In 1968 the TOW program was implemented with Automatic Test Equipment using hardwired controllers. This effort, while successful in achieving its purpose of mechanizing test operations, made evident that the use of custom designed controllers and sequencers entailed:

1. High non-recurring design and assembly costs

2. Long test equipment implementation lead times

3. Expensive modification when product requirements changed

Later implementations have taken advantage of the mini-computer technology which emerged in the early 1970's. It has been our experience that:

1. Mini-computers have proven to be a cost effective replacement for hardwired controllers in large and complex test systems.

2. Where the cost of these computers and their associated peripherals could be justified a decrease in non-recurring design labor and implementation lead times was achieved.

3. Use of mini-computers often means incurring additional costs above those required by the specific application because:

    a. Mini-computers, general purpose wide market instruments, contain more capability than necessary in test station controller applications.

    b. A significant effort is involved in integrating the computer system hardware and software into the test station.

4. Mini-computers and their peripherals, while small and rugged compared to large data processing systems, still require a significant amount of manufacturing floor space and must operate in a relatively controlled environment.

Due to our experience with hardwired and mini-computer automated test stations, we feel that the development of a low cost, test oriented controller based upon the new micro-processor technology should be undertaken.

To develop this low cost controller the manufacturing technology project would involve:

1. Defining the classes of functions now performed in existing automatic test system controllers

2. Determining the input/output and interrupt requirements

3. Formulating a modularized micro-processor based test system controller architecture

4. Developing a test oriented operating system environment with emphasis on "easy" interfacing to commercial equipment and custom electronics

5. Prototyping and testing of the low cost controller to develop performance/cost data for use in application trade-off analysis of new automatic test systems

Development of the low cost controller would produce the following benefits:

1. Existing automatic test applications can be implemented more economically.

2. The efficiencies of automation (reduced recurring labor and quantity of manual test positions required) can be expanded to manufacturing operations where current implementation costs now make the application cost prohibitive.

3. Reduction in the number of cables, harnesses, etc., since the controller can be built into, not connected to, the test system/product interface.

4. Decrease the non-recurring labor required for software development since the controller and its operating environment will be designed for test system applications.

5. Manufacturing floor space requirements for test systems will be reduced since the micro-processor based controller will be substantially smaller than current mini-computer systems.

The proposed modularized controller would be packaged on plug-in printed circuit cards (Figure 10). Due to the modular architecture employed, the number of circuit cards used in the controller (for additional memory, input/output and interrupt capability) will vary to match each specific requirement. In a typical application this proposed controller would be integrated into a product/test station interface; in this example, a circuit card test station interface adapter, Figure 11. We are currently using this interface adapter technique, with a mini-computer system performing those tasks which would be performed by the micro-processor based controller, and have found it to be a most effective approach for high rate, dynamic functional testing of electronic circuits. If the computation and control capability were placed within the product interface adapter (by using the modularized controller) it would be possible to simultaneously test a variety of electronic assemblies on a single test station. An example of such a test station is shown in Figure 12. While this approach can yield significant reductions in recurring labor cost, we have made no attempt to quantify these savings since they will be influenced by any operator interventions required (for adjustment, etc.) during the testing sequence.

Automated Fault Isolation

The second manufacturing technology project we propose is the development of an economically viable approach toward automatic fault isolation of analog electronic assemblies. This also encompasses the dynamic parametric testing (rise times, pulse widths, droop. etc.) of digital assemblies. If we take a look at where the costs lie in the operation of an automatic analog test station used in a manufacturing environment to test and troubleshoot products (reference Figure 13, Relative Cost of Automated Testing) it is readily apparent that the major contribution to recurring production cost is associated with fault isolation and diagnosis.

The use of an automated test environment as it stands today has shown that functional test failures which are detected in minutes or seconds require hours to diagnose, isolate and repair. This situation ties up large quantities of production assets in the expensive failure/repair loop because faults which are detected automatically are isolated manually.

In the future, as missile systems become increasingly more complex and component density escalates, the amount of production effort spent on fault isolation of defective product will become an even larger component of the recurring test costs unless effective new techniques are developed to automate troubleshooting.

Having analyzed the various approaches toward a cost effective method of automatic fault isolation of analog electronic assemblies, we feel that the most appropriate place to perform automatic fault isolation is on the same equipment which functionally tests the product and which detected the fault because:

1. The product is already on the test system

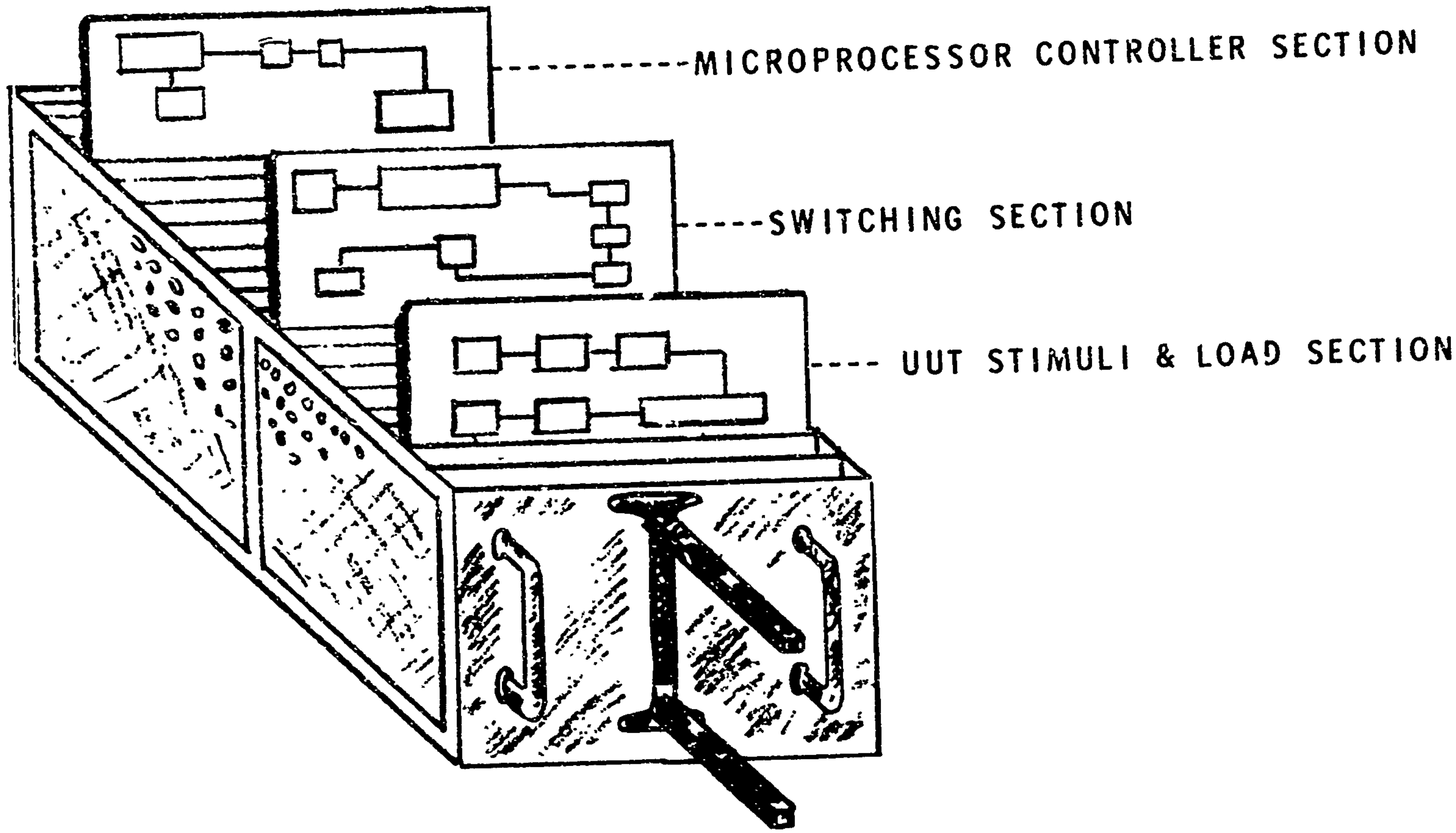
2. The functional pass/fail test results are at the test system

3. The stimuli and measurement hardware/software required to exercise the product are contained in the test system

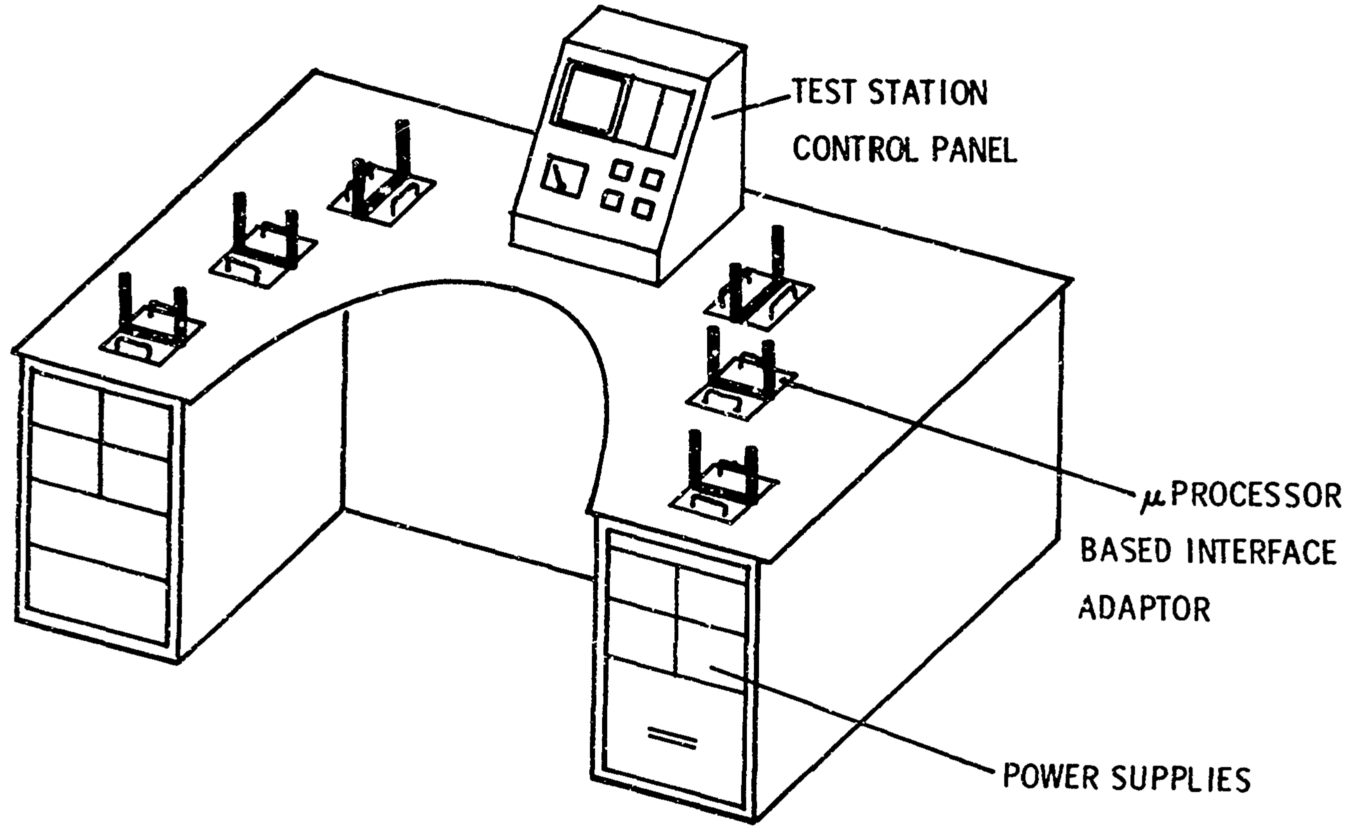
4. Fault confirmation problems will be eliminated

To perform fault isolation on a separate station would mean extra handling of the product, transfer of test data and costly duplication of test hardware and software.

(FIGURE 10)


MICROPROCESSOR CONTROLLER SECTION
SWITCHING SECTION
UUT STIMULI & LOAD SECTION

(FIGURE 11)

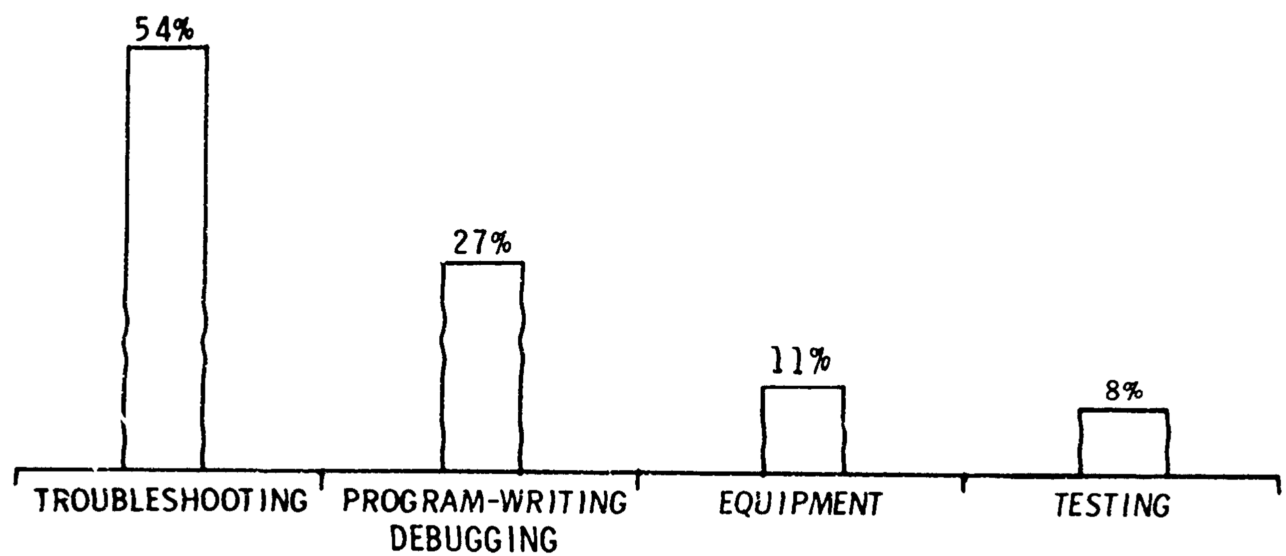


AUTOMATIC TEST STATION USING PROCESSOR BASED INTERFACE ADAPTORS

(FIGURE 12)

RELATIVE COSTS OF AUTOMATED TESTING

ANALOG TESTING



(FIGURE13)

This test station would be mini-computer or micro-processor controlled and would successfully isolate the fault area by using the functional test results plus measurements made on circuit nodes within the assembly. Since the ease and accuracy of troubleshooting depends on the test access available this project will encompass product probing techniques including the development of an automatic X-Y probe for circuit board fault isolation applications. Figure 14 depicts an automatic probe configuration which could be used in this fault isolation application. This device will not only speed up the probing operation but will also eliminate operator induced problems associated with probing an incorrect circuit node or remaining in contact with the circuit while the measurement is being made.

Accurate automated fault isolation will also require a comprehensive software package to determine the nature of the fault and which when aided by mechanized probing can rapidly locate the general area of the fault. At this point, possibly via circuit node comparison with reference standards, the probing system can be directed by the diagnostic routines to home onto the failed circuit element. This automatically operated system would eliminate operator mistakes which result in replacement of circuit elements determined defective due to erroneous fault isolation techniques. In addition to positioning the test probes, the automated fault isolation system would assure correct setting of test and measurement equipment controls. The main thrust of this investigation would be directed toward troubleshooting analog circuits. Development of fault isolation techniques for digital circuitry seems to be well under way by several prominent companies in the electronic equipment industry.

The specific tasks to be undertaken in the proposed manufacturing technology project are:

1. The investigation and cost trade-off analysis of the impact on product design and manufacturing costs associated with various test point access arrangements

2. The design and prototyping of different probing techniques and fixtures to eliminate the signal acquisition problems connected with the human operator

3. The development of a cost effective approach toward automating the decision processes in fault isolation signal analysis

4. The implementation of a prototype instrumentation and test system

5. The testing and evaluation of the resultant fault locstion and diagnostic methods to determine cost-benefit data

Development of this analog circuit fault isolation technology will produce the following benefits:

1. Reduce the recurring labor costs attributable to product troubleshooting of analog circuits by 40% to 70%

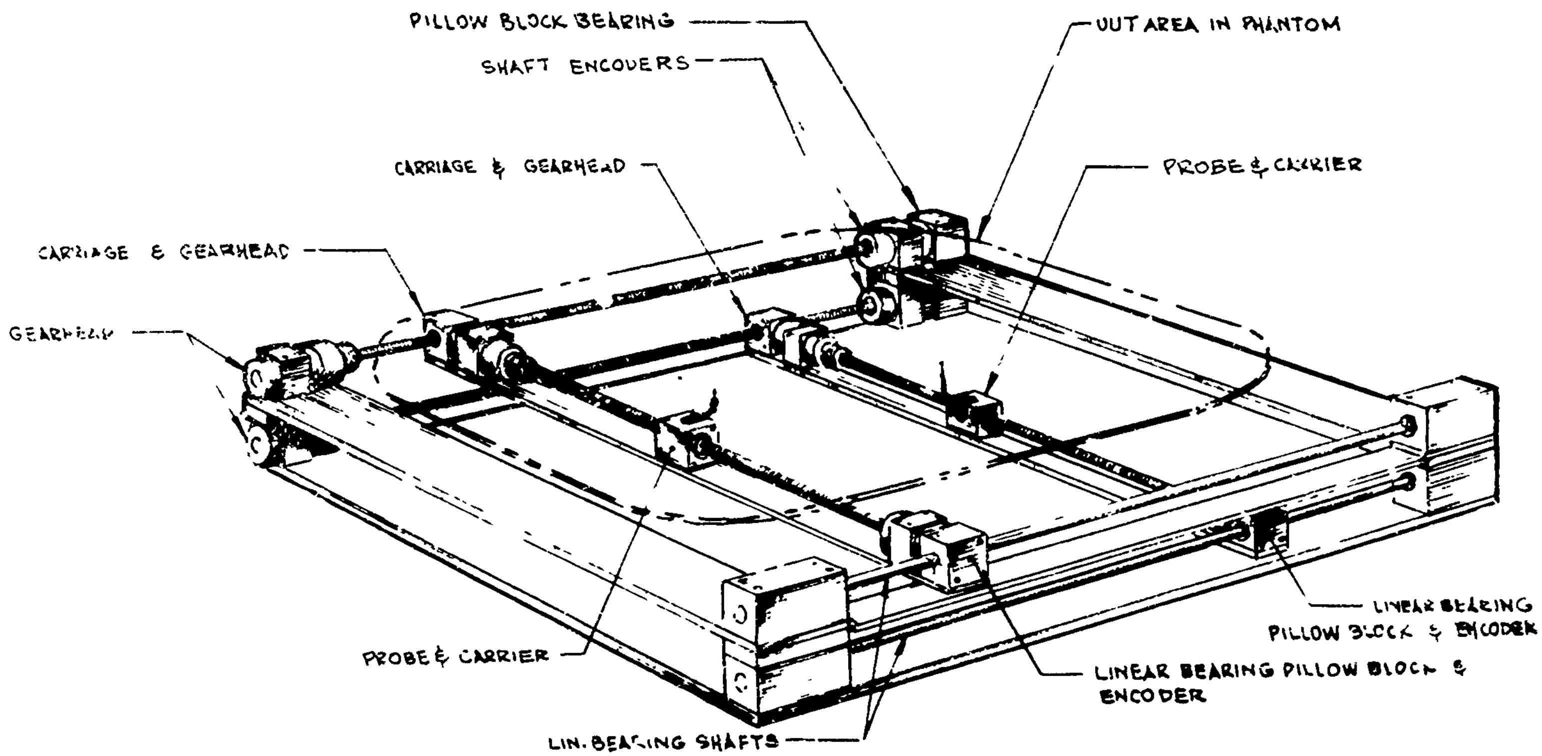
2. Direct reduction of high value production assets in the troubleshoot-rework-retest cycle

3. Reduction in the number of test stations required to support production since the same test system is used for functional test as well as troubleshoot duty

4. Fewer test/troubleshoot personnel will be required

5. Floor space requirements will be reduced due to fewer test stations

6. Rework and retest costs will be lowered because of more accurate determination of failed/faulty components


PILLOW BLOCK BEARING
SHAFT ENCODERS
UUT AREA IN PHANTOM
CARRIAGE & GEARHEAD
PROBE & CARRIER
CARRIAGE & GEARHEAD
GEARHEAD
LINEAR BEARING PILLOW BLOCK & ENCODER
PROBE & CARRIER
LINEAR BEARING PILLOW BLOCK & ENCODER
LIN. BEARING SHAFTS

(FIGURE 14)

SUMMARY

During this presentation we have analyzed as it relates to the manufacturing function, the criteria which determine what types of test equipment should be employed and the cost elements and cost drivers associated with both the implementation of test equipment and its subsequent use. In addition, the historical cost trend for test equipment implementation has been depicted as test technology progressed from manual to hard wire controller to mini-computer test systems.

Based upon this information, we have proposed two manufacturing technology projects: the development of a modularized micro-processor based test system controller and the development of a viable automatic fault isolation technique for analog electronic assemblies. These two projects, if undertaken, will allow the realization of significant reductions in both the recurring and non-recurring costs associated with manufacturing high quality, reliable missile systems.

PRODUCTION TEST EQUIPMENT TRANSITION

REDEYE TO STINGER

K. M. Wirgler

General Dynamics

Pomona, California 91766

ABSTRACT

The objective of this presentation will be to describe the transition from REDEYE to STINGER production. Emphasis will be on the improvement of the automatic production test equipment and the benefits derived.

INTRODUCTION

The REDEYE automatic production test equipment was controlled by a magnetic tape system. When developed in the mid 1960's, it was a very advanced type of automatic equipment. STINGER production test equipment will also be automatic, using the latest in computer control techniques. Improvements in test speed, overall functional capability, and cost will be delineated.

REDEYE SYSTEM DESCRIPTION

Introduction

REDEYE is a man-transportable, shoulder-fired, all Arms Air Defense System designed to provide combat units with the capability of destroying low-altitude hostile aircraft. The Weapon System is shown in Figure 1.

REDEYE Weapon

The REDEYE weapon consist of two principal sections: an Infrared Heat-Seeking Guided Missile and a Launcher.

Launcher. The Launcher consists of three main sections - Launch Tube, Sight Assembly, and Gripstock. It provides the gunner with a means of transporting, aiming, and firing the missile.

REDEYE Missile. The REDEYE Missile (Figure 2) is a rocket propelled, Infrared Homing (Heat-Seeking) Missile. It consists of five major sections: A Guidance Section consisting of a Seeker Section and a Control Section, Fuze and Warhead, Rocket Motor, and Tail Assembly.

The Seeker Section contains the Seeker Head and Electronic Assembly. The Seeker Section optically tracks the infrared energy from the target and supplies steering signals to the Control Section and the acquisition signal to the Launcher.

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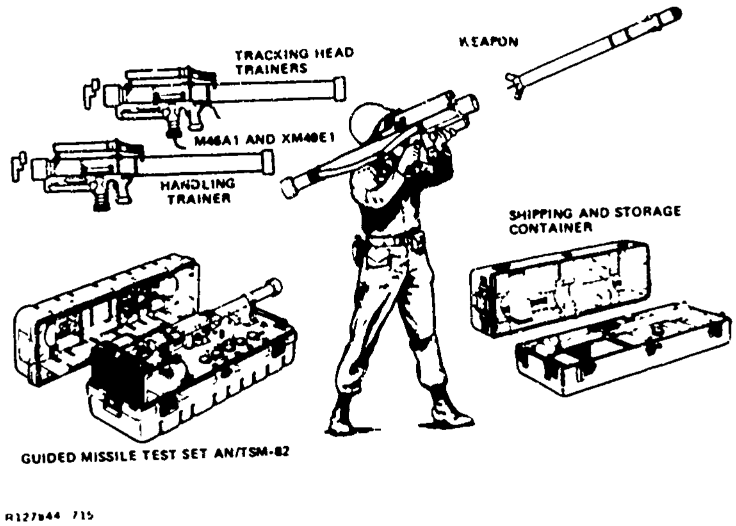
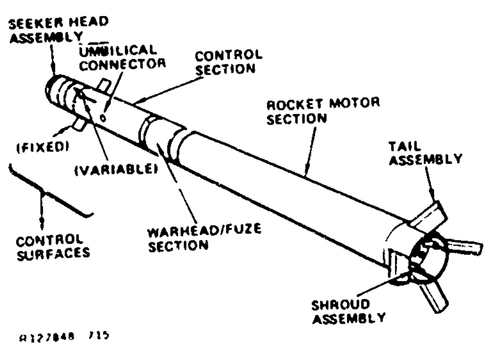


REDEYE Weapon System

Figure 1



REDEYE Missile

Figure 2

The Control Section is composed of an Electronic Unit and a Motor Driven Wing Assembly. Two pairs of fins, folded when the missile is in the launch tube, unfold and lock in place when the missile is fired. One pair locks in place while the other pair, moved by a set of gears and an electric motor, steers the missile in flight. The Electronic Unit provides the power and error signals for the steering motor. These error signals are converted to steering commands which steer the missile to the target.

Target destruction is provided by the Fuze and Warhead Section. All elements necessary for activation of the sustainer motor and arming of the warhead are contained in the fuze.

Propulsion for the missile is developed by a non-separating dual stage rocket motor section.

A Launcher Battery/Coolant Unit is used to energize the Launcher and missile electrical circuits and to cool the infrared detector in the missile seeker during the prelaunch sequence.

The REDEYE Guided Missile Test Set is used to determine the operational readiness of the REDEYE weapon and consists of a test unit with a freon gas bottle. The test set uses an outside power source. The following operational characteristics can be checked by the test set:

1. Missile response to an infrared signal.

2. Speed characteristics of the gyro in the missile.

3. Response of launcher acquisition indicator to infrared signals.

4. Alignment of launcher tube with sight.

REDEYE TEST EQUIPMENT

REDEYE test equipment, designed and developed in the mid 1960's, was a mixture of both automatic and manual equipment. The majority of the subassembly test equipment was manual while the assembly/section equipment was automatic. This report will focus on only the design approach, performance, and cost of the automatic stations which represented 65 percent of the total test equipment cost.

Major Test Requirements

Automatic test stations were required for REDEYE production to provide the most cost-effective compliment of equipment. Due to the high production rates, 1000 missiles sets per month, rapid and accurate testing of the hardware was necessary. This could only be accomplished with automatic test equipment.

Redeye Automatic Test Stations

Four REDEYE production automatic test stations were designed and fabricated. The automatic stations were:

1. P0202, Launcher Test Set

2. P0233, Board Assembly Test Set

3. P0203, Electronics Assembly/Section Test Set

4. P0207, Control Assembly Test Set

These automatic stations were magnetic tape controlled test stations and were very advanced equipment at that time. The stations consisted of a general purpose Master Automatic Programmer (MAP) unit common to all stations, a special purpose electronics rack and other special purpose equipment (Rate Tables, Roll Drivers, Cooling Units, etc.) to meet the unique requirements of each station. A general purpose block diagram is shown in Figure 3.

MAP Unit

The MAP, Figure 4, provides automatic control, measurement, comparison and data recording for all REDEYE production test sets classified as automatic.

In order to provide equipment with the maximum degree of standardization at a reasonable cost the MAP was limited to elements with a high use factor. With the board variety of signal switching and control requirements, the responsibility for test point selection and usage assignments for the control signals to be measured were limited to AC and DC voltage (0 to 100 volts), frequency (0 to 2 MHz), and time interval (10 microseconds to 99 seconds).

The use of eight bit 16 mm magnetic tape was selected as the input-output medium. The simple tape drive mechanism offered more reliable operation of the read-write portion of the system than the combination of paper tape punch and reader. Increased information density resulted in program tapes of approximately one eight the length of an equivalent perforated tape. This, in turn, allowed the use of simple continuous load cartridges rather than dual spool drives or complex cartridges for program handling. The same units could be used for both reading and writing. The magnetic tape usage also eliminated such problems as chad disposal and frequent lubrication of the short life punch and die sets.

Measurement. The Measurement Section of the MAP consists of three major chassis: (1) AC to DC Converter, (2) Voltage to Frequency Converter, and (3) Counter-Comparator Chassis. The block diagram of the Measurement Section is illustrated in Figure 5. The reversible counter was an in-house design capable of measuring frequency, time interval and frequency ratio. The counter also performed simple calcualtions.

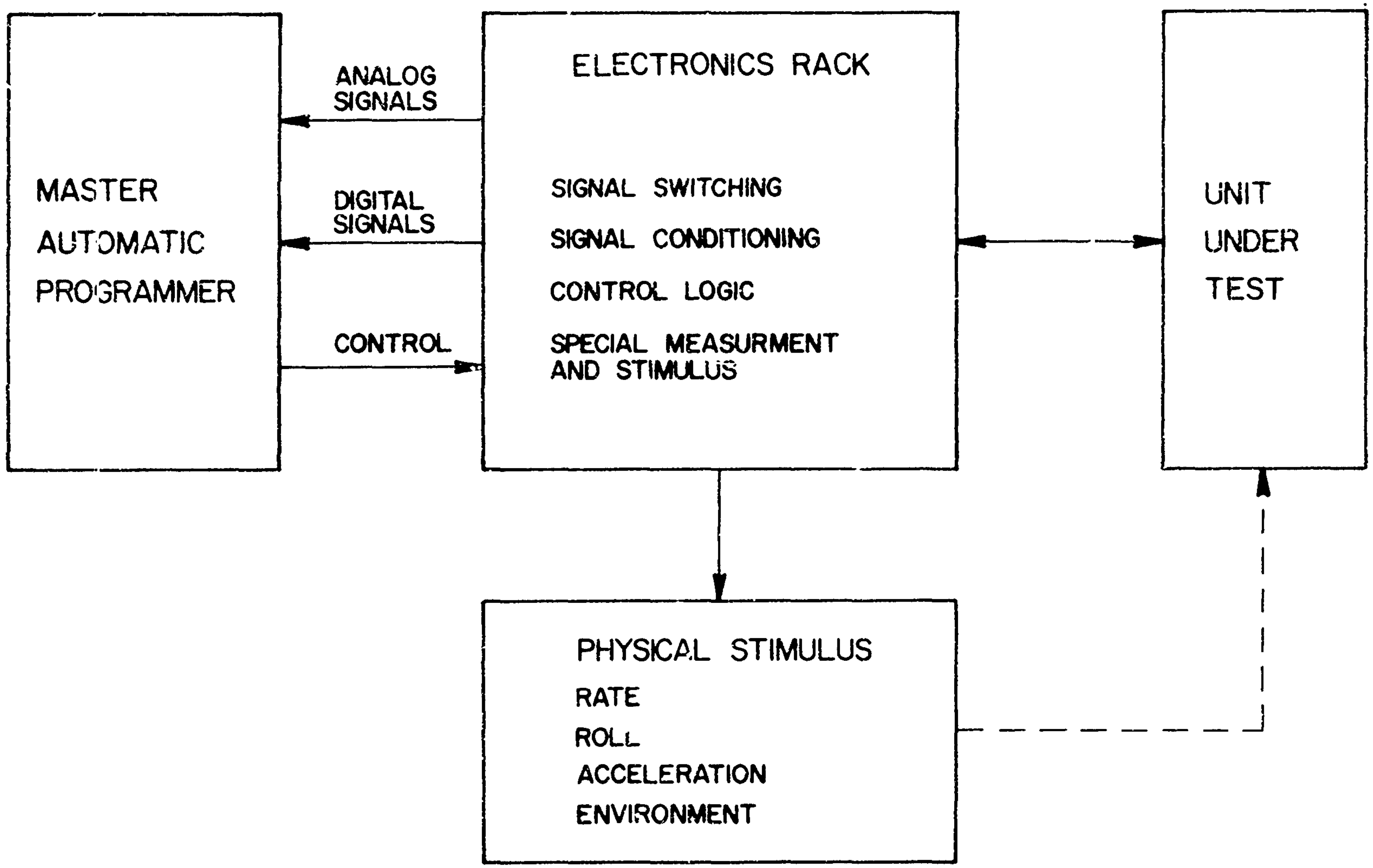
Program Tape. The program tape is of the length required to accomplish the tests allocated to the control of a single MAP system. It is possible to have several end item routines as well as the standard self-test and verification routines stored on a single tape and with the tape search feature automatically located the desired starting point.

Output Tape. The output tape is allowed to accumulate the recorded data for an eight hour shift, then is replaced. This tape is used to input data into a computer for parameter trend analysis and preparation of printed copies of the days' results for record purposes.

Test Stations

Each of the four automatic test stations interface a MAP unit. In addition, each test station provided a electronics rack containing its unique signal selection matrix, signal conditioning chassis, logic control chassis, unique stimulus and/or measurement instruments, and special interface circuitry. Each station also provides the required Unit Under Test (UUT) fixtures, Rate Tables, Target Simulators, Environmental Chambers, Cooling Gas, etc.

As an example, the Electronics Section Test Set, TE 0203 is presented. The test set performs complete evaluation of a Seeker or Guidance Section.

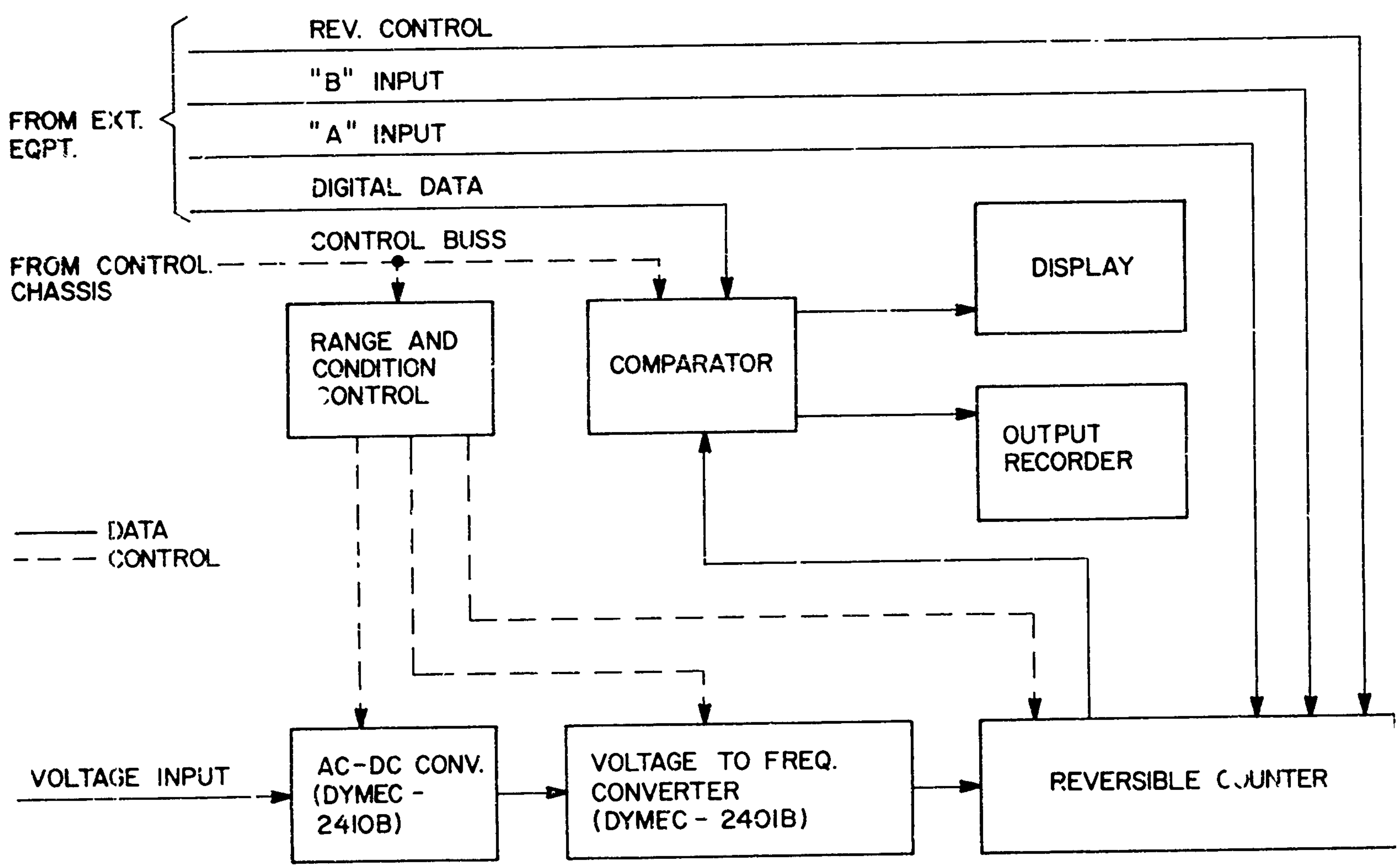


GENERAL PURPOSE BLOCK DIAGRAM,
REDEYE AUTOMATIC T.E.

FIGURE 3

MASTER AUTOMATIC PROGRAMMER (MAP)

Figure 4



M. A. P. MEASUREMENT SUBSYSTEM

FIGURE 5

The test set consists of the MAP, Electronics Section Test Assembly, Rate Table, and Vibration Stand. A floor plan of the test is shown in Figure 6. A TE 0203 station is shown in Figure 7.

The test set is required to perform the complete evaluation of a REDEYE Seeker or Guidance Section in approximately 17 minutes, and to indicate at that time whether the item is acceptable or not. This includes the time required to load and unload the test set (approximately 30 seconds). The test set is completely automatic with the exception of the load/unload operation. The Seeker or Guidance Section is installed in a fixture which is loaded into the roll barrel on the Rate Table. The Rate Table and all of the equipment on it are controlled by the Master Automatic Programmer. All the intermediate function control hardware is mounted in a three-bay cabinet assembly.

Figure 8 is a block diagram of the test set. It is a collection of basically independent subsystems. The interlock circuitry is the only common link between the subsystems. The digital information bus lines feed all decoding circuits in parallel.

STINGER SYSTEM DESCRIPTION

The STINGER Weapon System is under development for the U.S. ARMY and MARINE CORPS. It is intended as an eventual replacement of the REDEYE now deployed.

Like REDEYE, STINGER will be a light shoulder-fired weapon, whose mission is to provide low altitude air defense for forward area combat troops. To meet the air threat of the late 1970's and 1980's STINGER will have much higher capabilities than REDEYE. Although the guidance and propulsion of STINGER are considerably more advanced than those of REDEYE, the general principles of operation remain the same.

STINGER will be a certified round, requiring no field support equipment.

The STINGER weapon is shown in Figure 9. The notable difference compared to REDEYE is the absence of a Guided Missile Test Set. Based on the high availability experience of REDEYE, it is planned to treat STINGER as certified round. No testing is contemplated once the weapon leaves the manufacturers plant.

STINGER TEST EQUIPMENT

STINGER production test equipment is also a mixture of both automatic and manual equipment. The majority of the assembly/section equipment is automatic and represents approximately 60 percent of the total test equipment cost.

Stinger Automatic Stations

Four types of STINGER production automatic test stations will be designed and fabricated. The automatic stations are:

1. P0202, Launcher Test Set

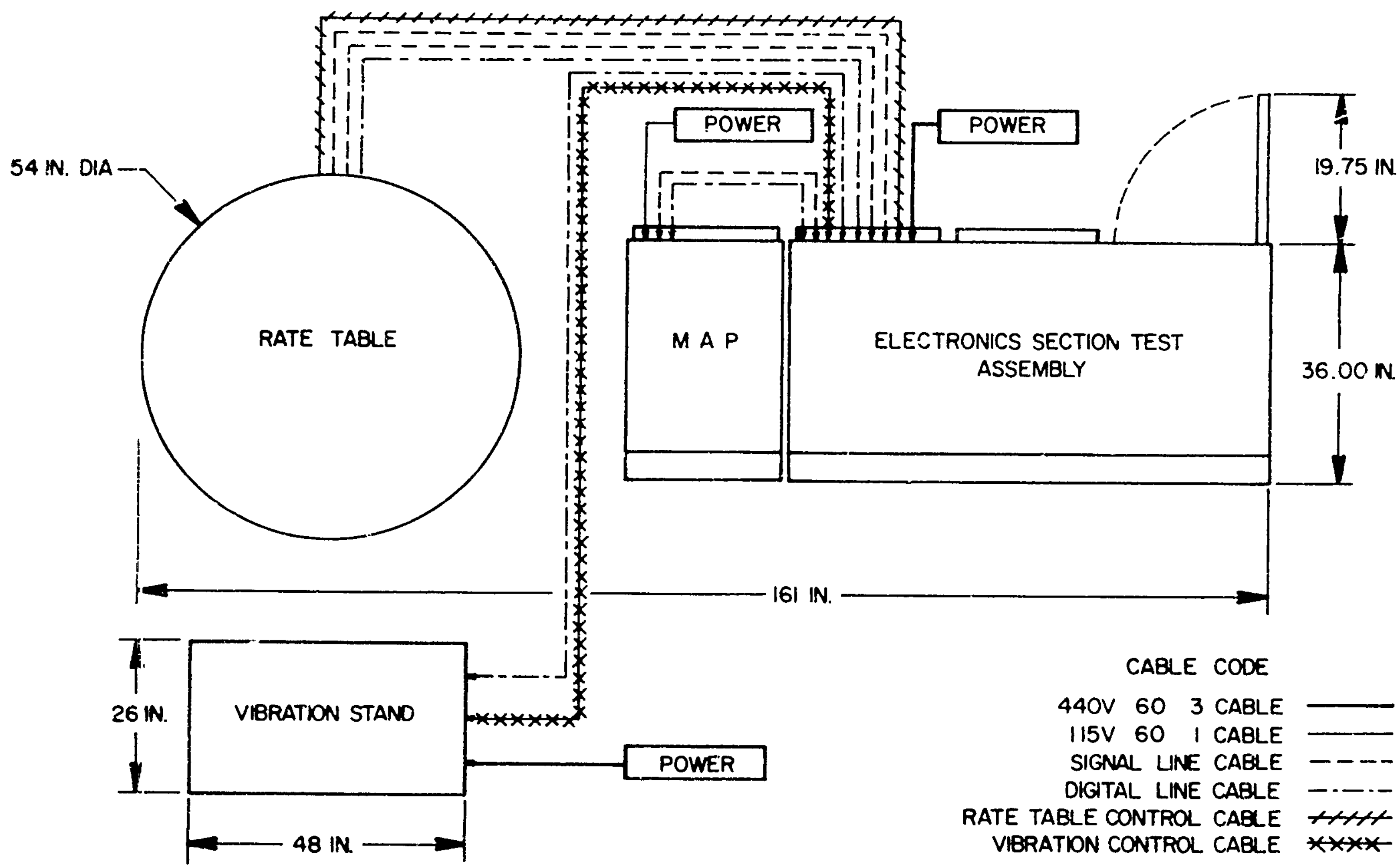
2. PS203, Electronics Assembly/Section Test Set

3. PS008, Board Assembly Test Set

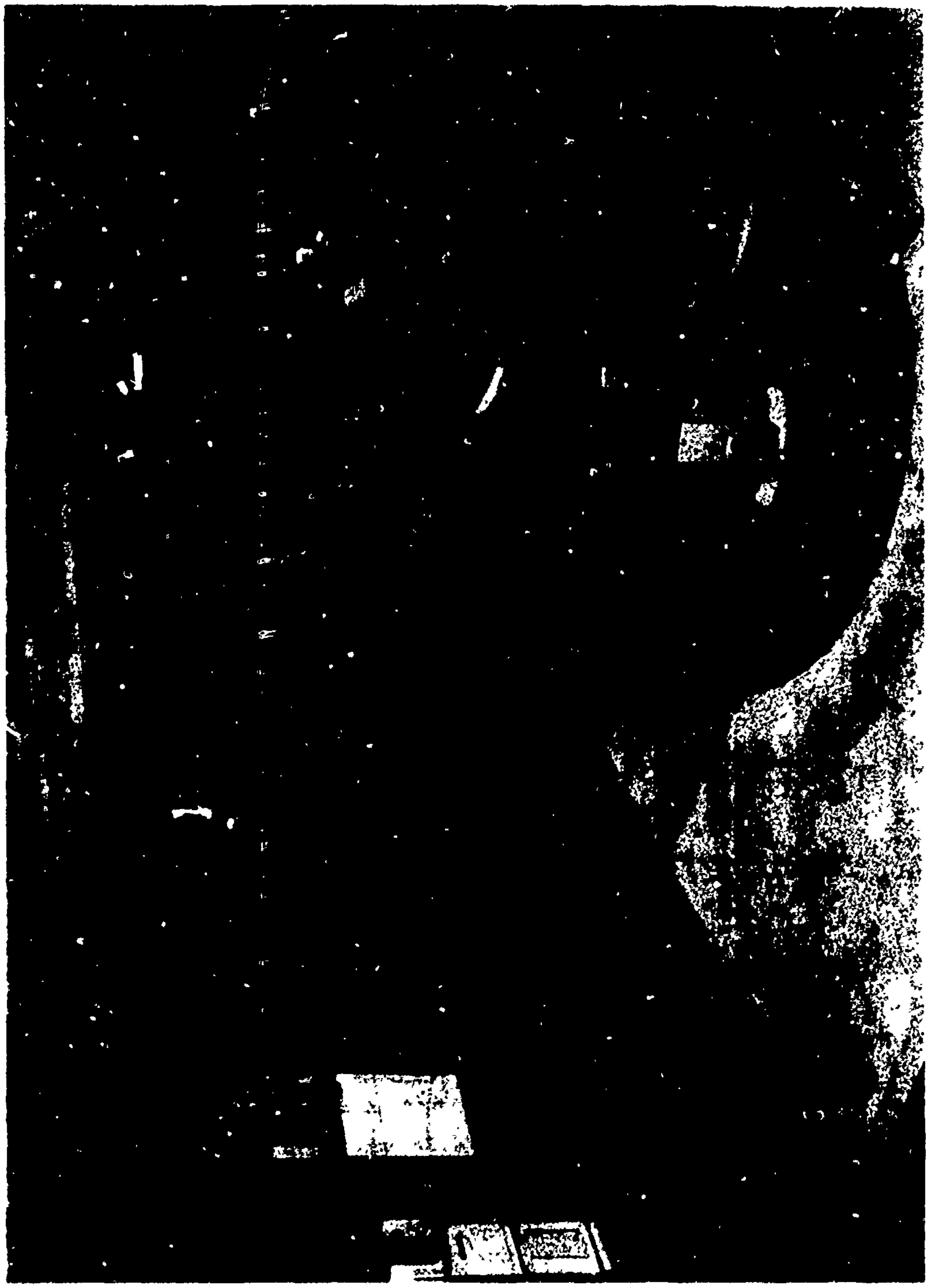
4. PS247, Control Assembly Test Set

General Description

The STINGER automatic production test equipment is based on a test system design that has evolved over the past five years. They reflect the latest design of standardized computer, peripherals, instrumentation and stimulus generation subsystems.



ELECTRONIC SECTION TEST SET FLOOR PLAN
FIGURE 6



A TE 0233 ELECTRONICS TEST STATION

Figure 7

BLOCK DIAGRAM ELECTRONICS TEST SET

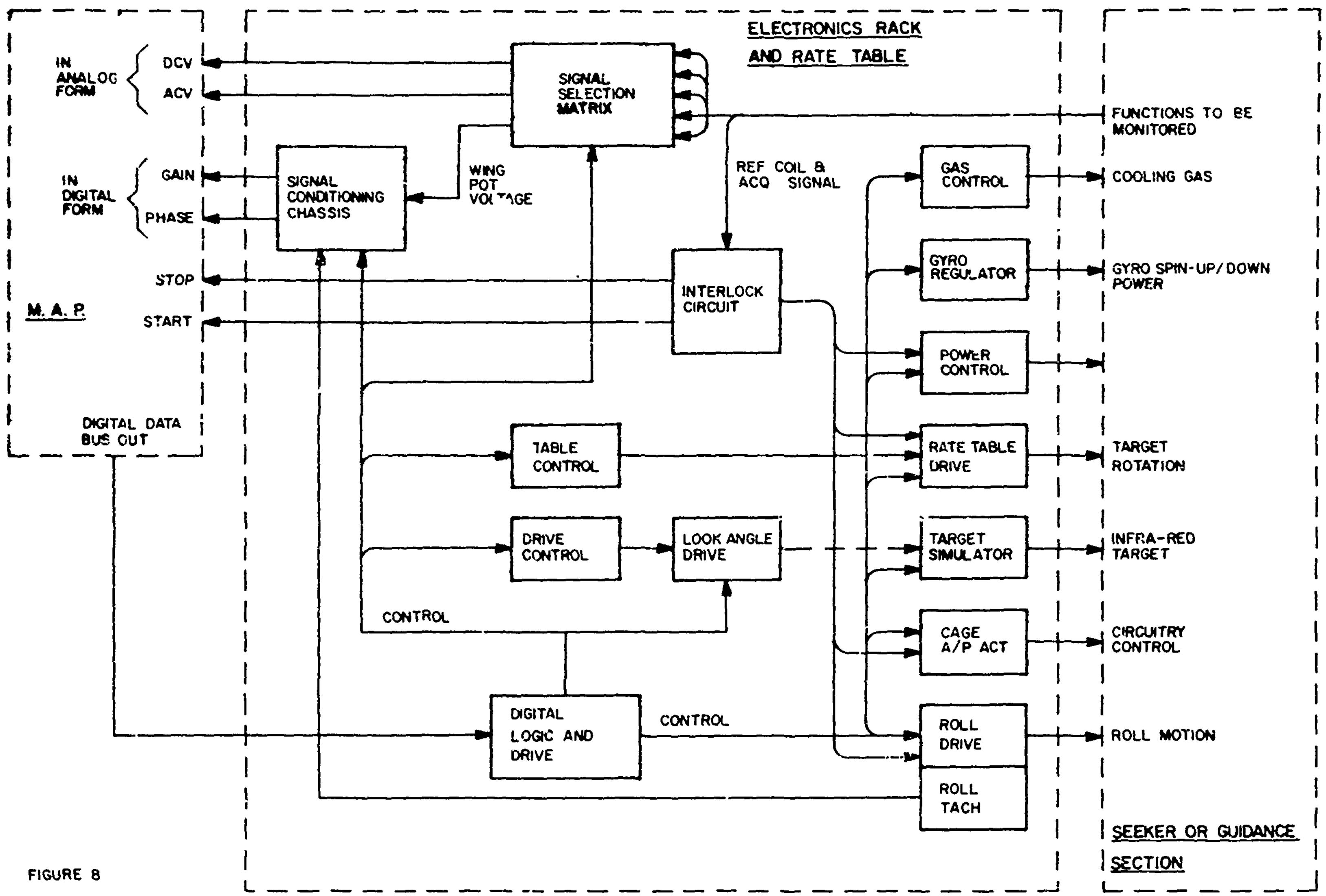
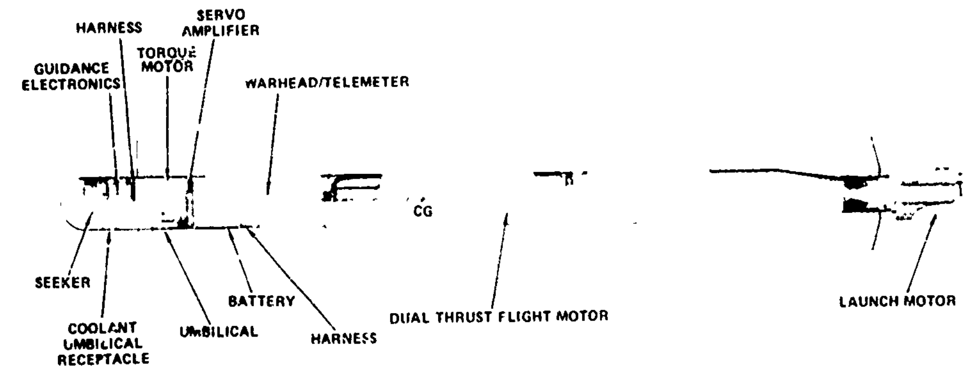
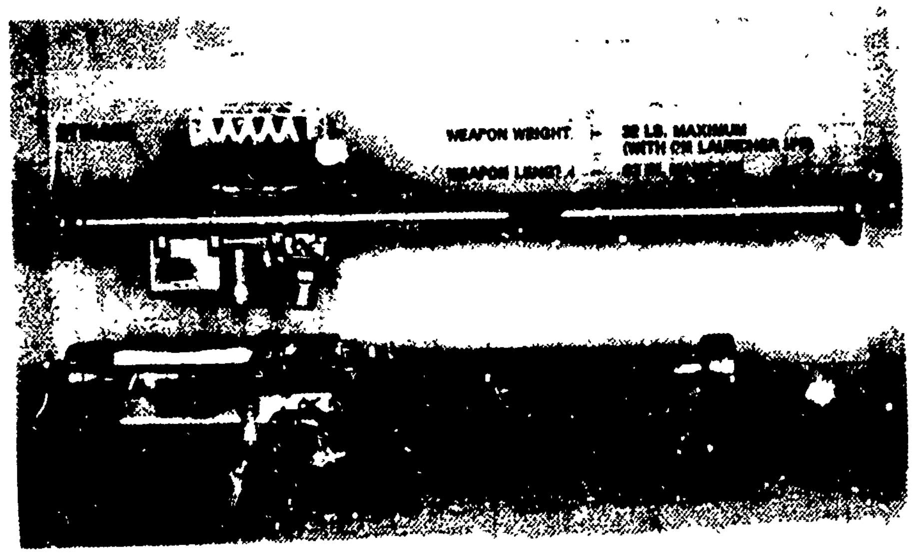


FIGURE 8





THE STINGER MISSILE AND LAUNCHER

Figure 9

A typical computer controlled test station consists of a "CORE" unit which contains the computer, peripherals, the general purpose instruments, stimuli, and switching required to perform the necessary functional tests.

All computer peripherals, test instrumentation, and station equipment are controlled through the Computer Subsystem. The Computer Subsystem comprises the computer, disc memory, Cathode Ray Tube (CRT), teleprinter, and line printer. The computer is a general purpose computer which uses up to 32K Core Memory to provide storage for the BASIC interpreter, TE instrument drivers and the test program being executed. This disc memory provides storage for test programs to be executed and for storage of subsystem routines. and test data. The CRT is the primary means of communicating with the computer. This terminal permits high speed readout and editing. The line printer provides hard copy printout at a rate of 100 characters per second.

The Instrumentation Subsystem includes items such as the system Digital Multimeter and Timer-Counter which are accessible through the Switching System. The Stimulus Subsystem includes AC and DC stimuli which are programmable to the UUT. The DC stimulus consists of accurate digital voltage sources. The AC stimulus can be either digitally generated by a Digital-to-Analog Converter or by a Programmable Function Generator or Synthesizer.

Special test fixtures, adapters, and physical and/or electrical stimulus units are interfaced with and controlled by the computer subsystems as required. A block diagram of a typical standardized automatic test station is shown in Figure 10. The final configuration of a test station depends on the unique test requirements for a particular station.

Test Stations

PS203, Electronics Section Test Station. As an example of the STINGER production test stations the PS203 is discussed. The test set will provide acceptance testing of the Missile Electronics Section. The Engineering PS203 is shown in Figure 11.

Peculiar Inspection Requirements. Testing and acceptance of the Electronic Sections requires the following major subsystems:

1. Rate Table Subsystem

   Provides rate and acceleration stimulus.

2. Roll Subsystem

   Provides three fixed roll rates.

3. Cooling Subsystem

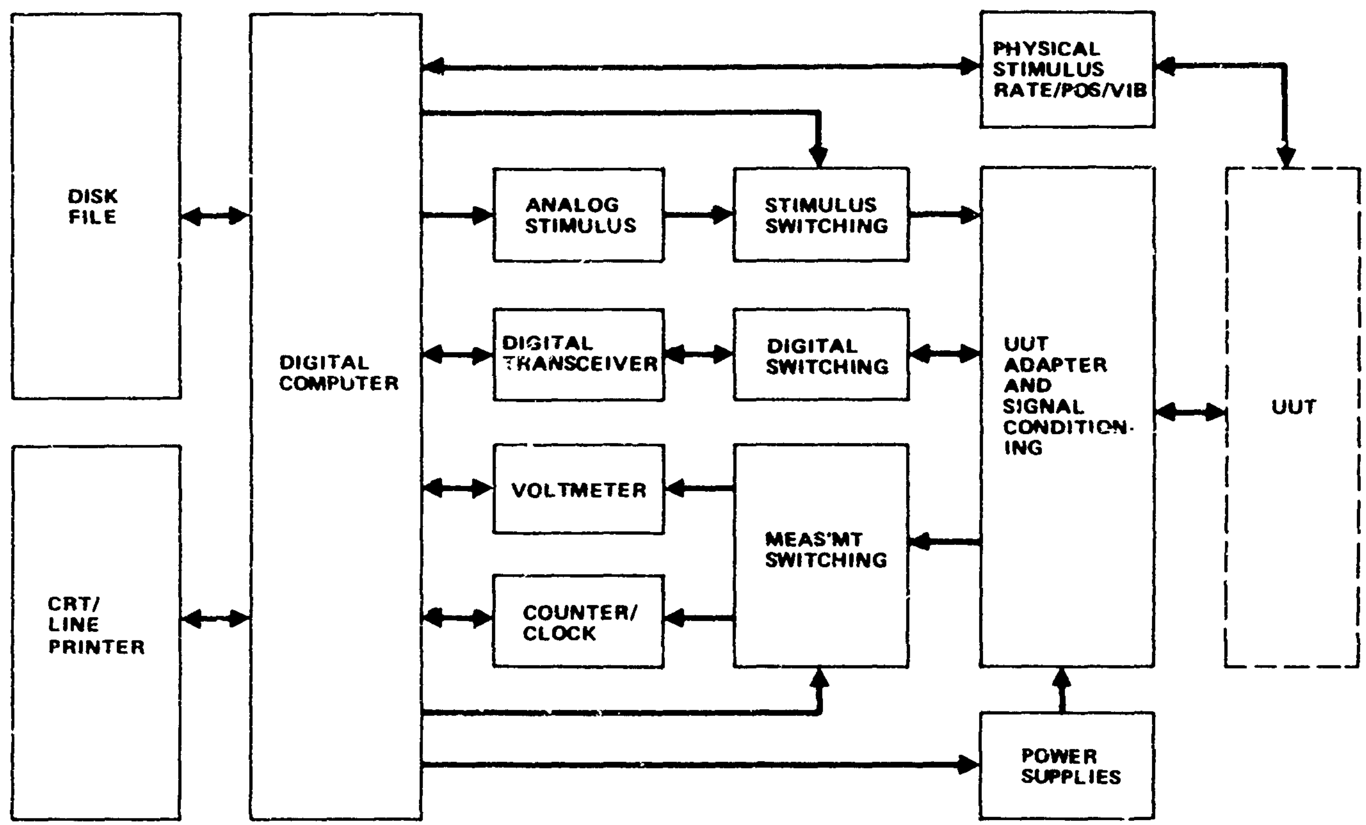
   Regulates and controls application of cooling gas at 3 different pressures.

4. Look Angle Subsystem

   Provides azimuth control of the target.

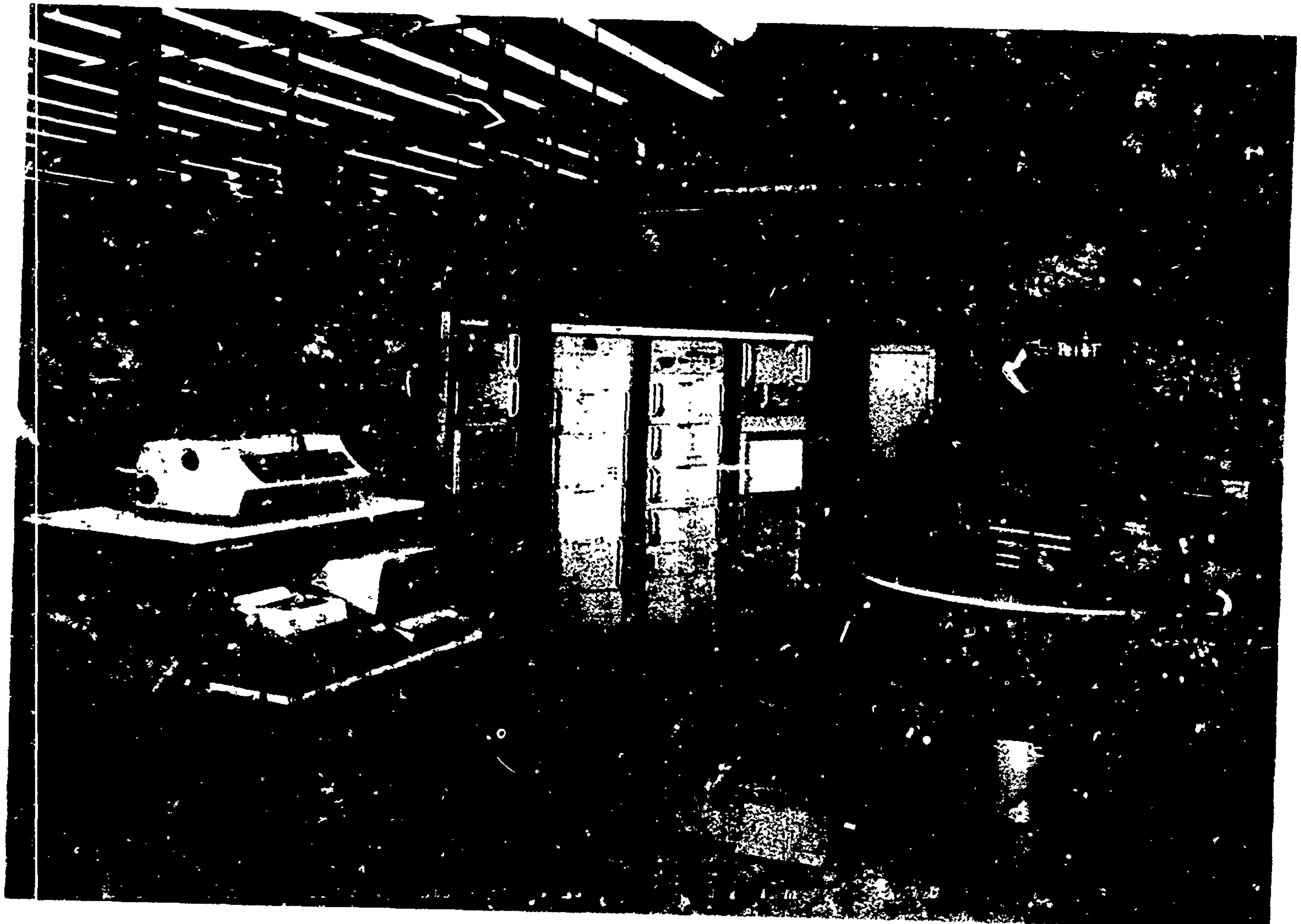
5. Target Select Subsystem

   Provides several target intensity levels. This includes an optical section, an IR source with a temperature controller and a filter/aperture mechanism.



BLOCK DIAGRAM GENERAL PURPOSE
COMPUTER CONTROLLED TEST STATION

FIGURE 10



P5203, ELECTRONICS SECTION TEST STATION

Figure 11

6. Gyro Drive Subsystem

Provides several selectable gyro spin frequencies in the normal gyro spin frequency range.

7. Gyro Spin Frequency Comparator

Senses the gyro spin frequency.

8. Measurement Subsystem

The following measurement modes are required:

1. DC Voltage

2. AC Voltage

3. Frequency

4. Time Interval

5. Phase

9. Unit Under Test, (UUT) Power/Control

UUT power supplies, current monitoring and special missile function controls.

10. Test Set and UUT interlocks to protect the item under test.

Although some of the major subsystems may be commerically available by themselves, for example the Rate Table Subsystem, other subsystems, for example the Target Control/Look Angle Combination, are unique and require considerable electrical and mechanical design and interface effort.

The overal integration of all the major subsystems and the development of an effective hardware/software combination require significant engineering effort.

These highly specialized subsystems and the overall integration are not commerically available and therefore Special Acceptance and Inspection Equipment is required.

Input Stimulus. Physical stimulus to the Unit Under Test (UUT) will be supplied by five test set subsystems. The Rate Table System will provide an accurate tracking rate to the UUT. The Roll System will simulate the normal UUT roll characteristic. A Look Angle System provides target azimuth positioning. The Gyro Drive System provides spin stimulus to the UUT gyro. Selected Infrared (IR) energy levels are provided by the Infrared Target System.

Direct stimulus to the UUT is provided by three test set subsystems. The Cooling System provides high pressure Argon Gas to cool the UUT detector. A UUT Power System is used to simulate battery power to the UUT. A UUT Function Control System is utilized to provide external control of certain UUT functions.

Output Measurement (Monitoring). Signal measurements will be made by a fast Analog-to-Digital Converter. Processing will be done via software.

The primary testing difference between REDEYE and STINGER is an appreciable increase in the quantity of parameters to be tested. Continuation of tape control equipment would have resulted in appreciable increase in quantity of test equipment for STINGER.

Computerized equipment was also less expensive as it consists primarily of standard commercial items whereas the tape system involved appreciable fabrication costs.

COST AND PERFORMANCE COMPARISON

Table I presents a comparison of the cost and performance capabilities of the REDEYE and STINGER automatic test stations. The equivalent hardware is tested on the stations. The stations can be compared as follows : P0202 - PS202, P0203 - PS203, P0207 - PS247, P0233 - PS008.

The total development cost for each REDEYE station (including test procedures and documentation) has been normalized to 100, an arbitrary figure. The total development cost of each STINGER station was compared to the appropriate REDEYE station. Thus, the total development cost of the STINGER PS202 station was 82 percent of the REDEYE P0202 station.

The normalized cost per parameter is only a figure of merit for each system. It can be seen from Table I that the cost per parameter has reduced considerably while total test time per parameter has also been substantially reduced. The reduction in cost per parameter is partly due to the substantial price reduction of test equipment computer and peripheral hardware and partly due to a standardized equipment design. Test time per parameter is reduced primarily due to the speed advantages enjoyed by computer controlled testing. The reduction in test times is typically limited by the unit-under-test response time.

Another cost benefit provided by the computerized STINGER test equipment was a reduction in hardware costs by utilizing software techniques. As an example, REDEYE required a $10,000 phasemeter. In STINGER equipment the same function is performed in software in conjunction with the voltmeter. This method completely eliminates maintenance costs and improves system accuracy.

STATIONS	NORMALIZED/COST	NO. PARAMETER TESTED	NORMALIZED COST/ PARAMETER	TOTAL TEST TIME, HRS.	TIME/PARAMETER, SECONDS
			Redeye		
P0202	100	33	3.03	.23	25.0
P0203	100	81	1.23	.78	34.7
P0207	100	74	1.35	.29	14.2
F0233	100	159	.63	.64	14.4
			Stinger		
PS202	32	94	.87	.15	5.7
PS203	44	101	.44	.33	11.8
PS247	86	194	.44	.38	7.1
PS008	81	211	.38	.27	4.6

Cost and Performance Comparison, REDEYE and
STINGER Automatic TE

Table I

TEST EQUIPMENT COST DRIVERS

The previous section presented the cost of each major STINGER automatic production test station compared to the equivalent REDEYE automatic test station. This section presents the detail cost elements of the STINGER automatic stations. The "average" costs, shown in Table II, for the four STINGER automatic stations are expressed in terms of percentage of the total station cost.

Table II shows that the major hardware cost elements are the Stimulus, Measurement and Data Processor Subsystem. UUT test procedures and documentation are the major software cost items. These are average costs since they will vary from station to station depending on the unique test repuirements.

Documentation

Test equipment documentation, drawings, are the major nonrecurring cost elements. This was true with REDEYE and will also be true for STINGER production test equipment. Appreciable cost reductions could be achieved by greater use of commerical type documentation.

Procedures

Another major cost category, but one that may no be fully appreciated, is the cost for UUT test programs. This includes, primarily, the time to write and evaluate the test programs. The cost is obviously proportional to the number and complexity of the UUT's and parameters to be tested. Although automatic test systems continue to become more powerful and test programs easier to develop and edit (through on-line CRT program development and editing) missile hardware also continues to become more complex with more parameters to be tested. The net result is that programming costs continue to be a major cost item. Standardization of a programming language, such as ATLAS, throughout industry will help reduce these costs.

Hardware Subsystems

The Stimulus, Measurement, and Data Processor Subsystems represent substantial cost elements of a test station since they are typically outside purchased parts (signal generators, voltmeter, computer, etc.). OSP items, especially computers and the associated peripherals, have experienced substantial cost reductions the past few years while at the same time drastically improving performance capability. This trend will continue, especially as microprocessors become more powerful and influence computer and instrument subsystems. Another trend reducing hardware costs is the use of more powerful system software when used in conjunction with in-house designed sampling-measurement and arbitrary function generator systems, to replace OSP instruments.

Another major cost element for the STINGER test equipment is the Target Simulation Subsystem. The purpose of an infrared target is to provide, to a Heat-Seeking Missile, a realistic simulation of target parameters. The IR target provides the capability to checkout the missile performance under controlled enviromental conditions. The Pomona Division of General Dynamics has placed great emphasis on providing improved target presentations throughout the development cycles of the IR Seeking Missile.

Other stimuli/input equipment is provided for STINGER. The missile is rolled and presented targets at various look angles. Tracking is introduced by mounting the Target Roll Assembly on a precision rate table. Other environments provided are acceleration (g's pulled by the missile), wideband vibration, high temperature, and low temperature.

SUBSYSTEM (COST ELEMENT)	MATERIAL	PURCHASED PARTS	PROCESS & FABRICATION	ASSEMBLY	TEST & INSPECTION	SUPPORT	% PRODUCTION COST
HARDWARE							
Stimuli System	20	60	8	4	4	4	10
Measurement System	10	70	6	6	4	4	8
Power System		80	10	2	4	4	2
Control System	50		20	20	7	3	3
Environmental Control System	5	80		5	5	5	3
Data Processors		87		5	4	4	10
Switching Networks	30	10	30	10	15	5	3
Special Panels/Displays	5	80	5	5	3	2	1
Cables/Harnesses	20		45	17	10	5	3
Enclosures/Racks	30		25	20	3	2	1
SOFTWARE							
Executive						100	6
Unit Under Test						100	15
Documentation						100	35
							100%

Test Equipment Cost Elements

Table II

Cost Minimization

As mentioned previously the computer controlled test station "CORE" unit is a standardized design. Thus, a minimum design cost for new computer controlled stations is achieved. The major test station design costs are realized to provide the unique interface requirements of the UUT and the required simulators and/or external stimulus or measurement instruments (rate tables, gas cooling, etc.).

Another possible long term cost reduction is the standardization of the programming language ATLAS for computer controlled test stations. A transistion cost to switch to a new UUT programming may result, but long term advantages will be possible from the use of a common language throughout the industry.

REQUIRED PRODUCTION TECHNOLOGIES

The manufacturing technology project of designing and developing prototype production test equipment during the engineering development stage of a project was implemented in both the STINGER and Standard Missile 2 (SM-2) engineering development programs. This has lead to our current design of computer controlled equipment planned for both of these production programs. The advantage of this approach will be reduced TE developed costs, improved system performance, and reduced lead time for the production test equipment.

Other manufacturing technologies have been in the development process in industry for many years. A very important area, one that may substantially reduce recurring production cost of missile hardware, is fault isolation of both analog and digital boards.

Impedance Testing

Impedance testing has been available for several years and continuing improvements in these test systems have made them very effective in locating faulty circuitry card components. To evaluate impedance testing of analog circuits as a means of fault isolation a comparison of this technique with current factory methods was conducted at General Dynamics.

The existing production fault isolation equipment is manually operated TE with stimulus, power supplies, and measuring devices which are rack mounted and accessed through the control panel and test fixture. Functional fault isolation is performed using signal tracing techniques. The impedance tester used was an automatic station with access to 2-D boards through a vacuum-assisted test fixture via spring-loaded test probes. The board under test is pulled down on the test probes by the vacuum.

Based on a production rate of 200 missile systems per month the study showed a projected savings of approximately 100 hours per month in fault isolating STINGER circuit boards.

Digital Fault Isolation

Complexity of current logic circuits have made test program and subsequent fault isolation a formidable task. The selection of a digital logic tester and program preparation method is a complicated task. It depends on the volume of boards to be tested, the variety of board types, characteristics of boards, and the effectiveness of later system test. The prime concern is how much it will cost to test or not test boards over a given period of time.

The important point is that impedance testing and digital logic fault isolation techniques may substantially reduce the recurring cost of circuit board repair. Many times these capabilities are not considered necessary and to reduce the initial production development costs these capabilities are eliminated from the bid.

Hardware and Software

To further reduce TE material costs more testing and analyzing may be accomplished with improved system software. As sample-data-systems and arbitrary function generation capabilities improve more measurements and analysis will be accomplished through software and use of fast fourier transform techniques.

COST TRENDS

As shown in the "Cost and Performance Comparison" section of the presentation two factors became apparent. First, missile hardware is becoming more complex. This is identified by the fact that the total number of parameters to be tested for common REDEYE and STINGER hardware has increased. Secondly, the total test system cost per parameter tested is decreasing. This has partly been about by technical advances, such as order-of-magnitude increases in speed and memory capacity, and also order-of-magnitude reductions in cost of computer systems over the past several years. Although the cost of computer subsystems is still dropping, it is decreasing at a much slower rate. Relative costs of software is now beginning to increase.

Digital fault isolation capability is an area that will provide considerable cost savings to production programs. This is an area that is more difficult to quantify due to the problems in obtaining fault isolation data. New techniques have been developed which will allow for the cost-effective generation of digital fault patterns and probe tracing for digital boards and modules.

Title: Manufacturing Technology Project To Reduce Recurring Fault Isolation Cost Of Circuit Boards.

System Panel Area/Component: STINGER/test equipment/fault isolation.

Problem. Manual fault isolation of STINGER circuits cards is potentially very expensive. The use of computer controlled stations to perform impedance testing on the circuit cards could save as much as 100 hours per month of manual fault isolation time.

Proposed Solution: As a minimum this project would provide for the addition of impedance test capability to the STINGER circuit board test station. The task would include hardware design and integration of an impedance test, preparation of control software, and the preparation of test procedures.

Project Cost and Duration:

Design	$ 12,000
Hardware	35,000
Software	8,000
Test Programs	40,000
TOTAL	$ 95,000

Estimated duration of the project is eight months.

Benefits: Benefits to be derived from this project are a reduction in recurring fault isolation costs. The technology porject could also be applied to other missile programs. The reduction in cost for stinger could be up to 100 manhours per month for fault isolatiom time, assuming a production rate of 200 missiles per month.

TEST EQUIPMENT COST DRIVERS AND THEIR FUTURE TRENDS

O. T. Carver and J. H. Groff

RCA Corporation

Burlington, Massachusetts 01803

ABSTRACT

A contemporary test equipment supporting Army missile systems is used as a basis for cost element derivations and cost/technology trends. The Land Combat Support System (LCSS) is a test and repair system in use with several Army missile systems. LCSS supports four forward area tactical missile systems; the Shillelagh, TOW, Lance and Dragon in the field and, to a limited extent, the Depot environments. The significant cost factors include both hardware and software elements. The general purpose capability spreads the hardware cost across a number of applications, and as an automatic test equipment, software costs are a function of the number of missile system items tested. Technology advances since the era of LCSS design are tending to (1) reduce recurring hardware costs by trade-off for one-time software investment, and (2) develop automated test design techniques for the application software.

INTRODUCTION TO LCSS

Purpose

The Land Combat Support System is a common support equipment for missile systems possessing varied tactical and technical characteristics. It was conceived to provide maintenance support for major assemblies and subassemblies of the Shillelagh, TOW, Lance and Dragon missile systems. Although its primary purpose is for direct and general support missions, LCSS is suitable for use at Depot when augmented with acceptance and inspection equipment. The primary objective of the LCSS design was to provide automatic, multisystem test equipment capable of supporting in the field any land combat missile system and also be capable of self support. The variation in characteristics of the missile system can be seen from Figure 1.

The Shillelagh missile system is vehicle mounted, uses an IR guidance link, and the guidance system is housed in seven major assemblies. The missile itself is not repaired in the field. The TOW is man portable, uses an IR tracker but the guidance link to the missile is through wires trailed from spools on the missile. The missile, as with Shillelagh, is not repaired in the field. Lance is a point-to-point weapon using a modified inertial guidance system. Both the missile and the pre-launch equipment are field repairable. LCSS came into being as a multisystem support equipment scaled to the Shillelagh,

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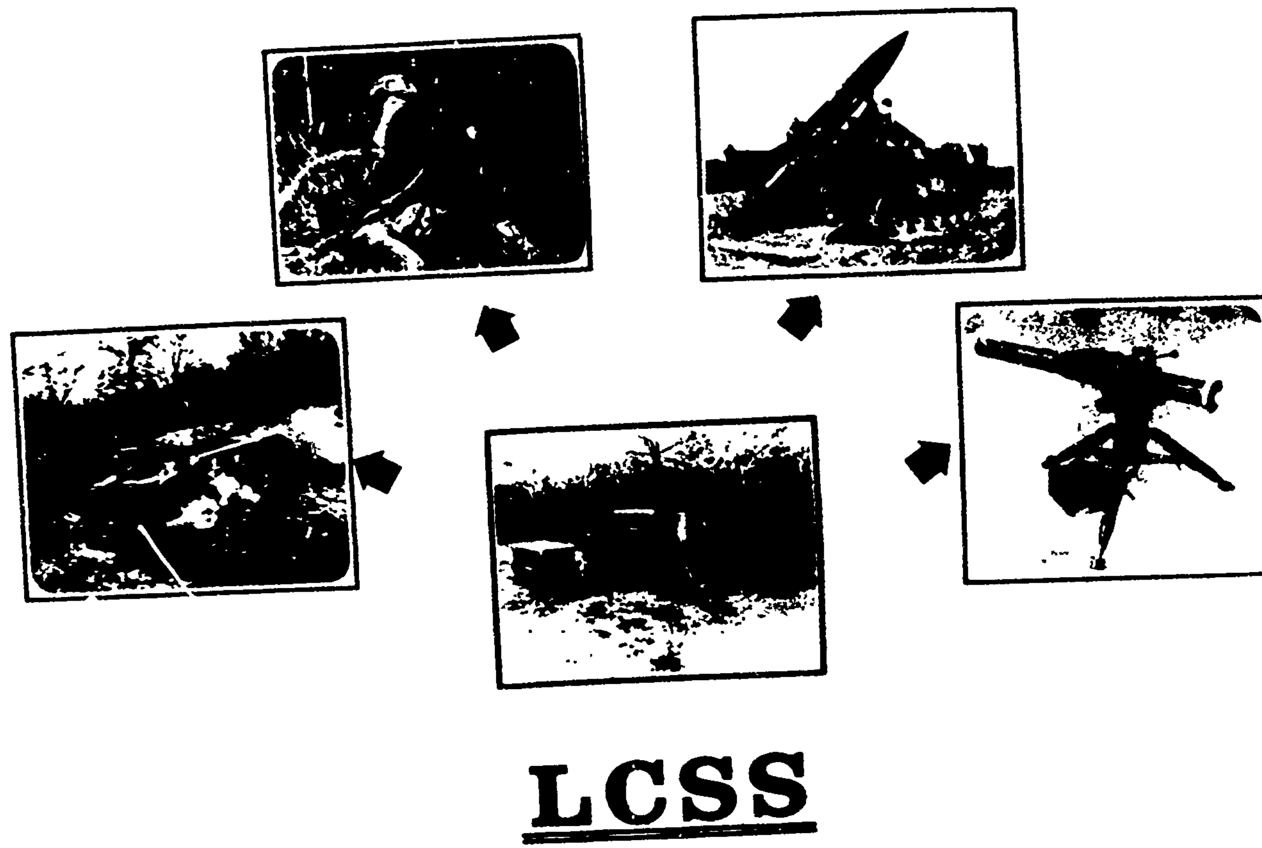

Figure 1. Missile System Characteristics.

Lance, and TOW support requirement. Later, Dragon was added to the LCSS support requirements.

LCSS is a two-shelter system with the automatic test set in the first shelter (AN/TSM-93) while the second shelter (AN/TSM-94) provides repair and storage functions.

SYSTEM DESCRIPTION

Figure 2 shows the two shelters, cut away to show the test set operator's console and electro-optical test position. As shown, the shelters can be used from the back of the transporting truck or can be placed on the ground.

The LCSS is designed for transport by cargo aircraft, standard wheeled military vehicles, and by helicopter. Total weight for each shelter with equipment is approximately 6000 pounds. Each shelter includes an integral heating-cooling system which allows continuous operation throughout the global environments.

Integrated circuits are used in all control and digital applications, and this has made possible the relatively small size of the test equipment. There are two test stations and one repair station in the shelter plus storage for test tapes, cables, and adapters.

The automatic test system consists of a controller/data processor, input/output measurements, electronic stimuli, switching, adapters, and internal power. The controller/data processor subsystem provides the interface between the input/output and the remainder of the test set. It accepts programmed data from either the perforated tape reader or the manual input and uses this data to control the operation of the stimuli, measurements, and switching. It also accepts measurement and control data and performs algebraic addition and subtraction computations as required to determine the operational readiness and/or faulty components of units under test (UUTs).

The input/output function provides the inputs necessary for system operation as well as the outputs required by the operator. The measurement subsystem has the capability of performing frequency, time-interval, peak-voltage and resistance measurements. It receives inputs via the switching function from the UUT and from selected self-test points in the test system. All these signals, whether DC, AC, or resistance, are converted to a binary coded decimal (BCD) quantity which is then routed through the controller/data processor for further processing and for decimal display. Self-test of the measurements subsystem is accomplished through the use of internal reference standards. Both AC and DC voltages from the stimulus subsystem provide both signal and power stimuli to the UUT. The DC voltages are programmable in amplitude; AC signals are programmable in amplitude, frequency and waveform characteristic. Available to the Shillelagh transmitter UUTs are special stimuli supplied by Shillelagh modulator assembly (GFE). Self-test of the electronic stimuli is accomplished by routing the stimuli to the measurements function. The source and detector adapters form a subsystem for test of electro-optical devices.

The switching provides the interface between the UUT and the remainder of the test system. Through test connector panels and under program control, signals to be monitored are routed to the measurement function. Special handling of sensitive UUT signals may be accomplished by the use of probes located on the measurement assemblies.

An external engine-generator set furnishes three-phase, four-wire power with a line-to-line voltage of 208 VAC at a frequency of 400 Hz. This prime power is supplied through

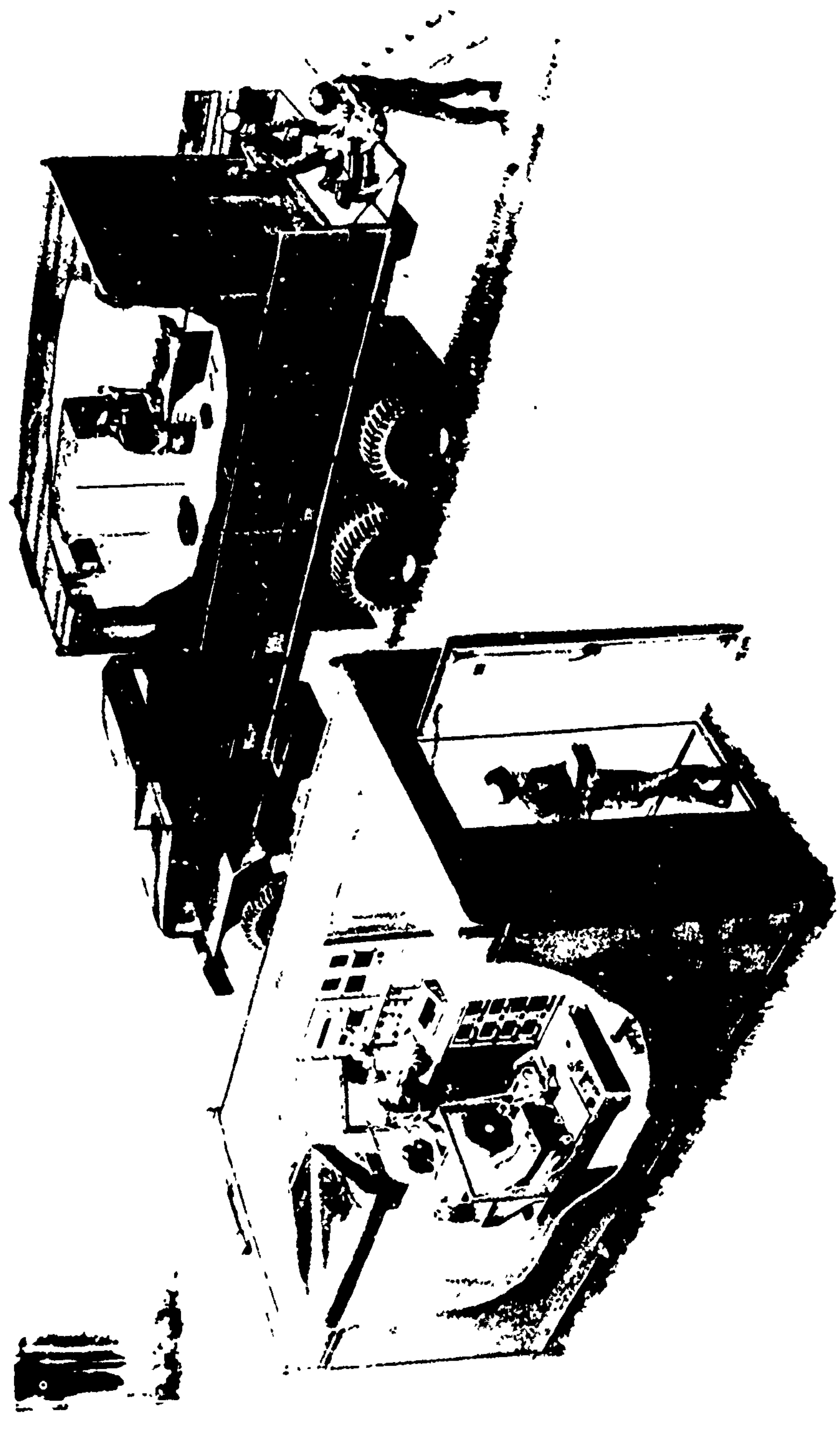

Figure 2. LCSS In The Field

the power distribution panel.

PROGRAM STATUS

LCSS is presently deployed world wide. The original system design studies were initiated in 1964, followed by developmental models and test demonstrations on Shillelagh, Lance and self-test programs during 1965 and 1966. In 1967, four service test models were delivered, and military operator and maintenance personnel training was started. The first initial support sets were deployed in 1968 in support of Shillelagh at Fort Knox, Kentucky. The same year the first of the engineering test/service tests at White Sands were completed and LCSS was committed to production.

Counting the three developmental models and four service test models, all of which are still in use, there are over fifty LCSS systems delivered.

Test Software

Programming software was, from the beginning, an important part of the LCSS program. In fact, Army acceptance of overall hardware/software development was based on demonstrations of test programs running on LCSS in test and diagnosis of UUTs. The contractor's fee was determined by the ability of the overall test system and its software to detect faulty units under test and to diagnose failures to the source of failure. It was expected that the test system would, in 99 percent of the cases, identify good units as good and bad units as bad. The LCSS contractor had to correctly locate UUT faults in 90 percent of the test cases in order to achieve target fee. Above 90 percent he earned fee up to a maximum at 96 percent and over. In more recent contracts the condition for acceptance of the test program is demonstration of better than 90 percent correct diagnostic capability.

In retrospect we know of no better way to demonstrate acceptable ATE systems than to require test/diagnosis demonstrations of the hardware/software combination. The faults were determined by the Army based on failure mode analysis of the individual UUTs and were, of course, not made known to the contractor prior to the demonstration test. Knowing the conditions of acceptance, the contractor instituted a strict series of software design reviews and sampling tests during validation to increase his confidence in the individual test programs before submitting them for acceptance.

An assembler, called ASEIP for Assembly Static Error Inspection Program, was developed early in the LCSS program as a software aid to test program development. Later, lessons learned with ASEIP were applied to the development of UTEC or Universal Test Equipment Compiler. UTEC is being used for new test program designs and program updates.

As a general purpose maintenance tool, LCSS in development had an interface with the weapon system prime equipment manufacturers and with various project offices within the Missile Command. The missile system prime initially developed the test designs based on test requirements for the items under test and help from the LCSS contractor relative to test equipment capability and interface.

As a result of the experience with the Shillelagh test programs, a different philosophy was developed for the TOW assembly programs. Under the previous split responsibility philosophy, there was no penalty if the test program did not find a fault because of missing

logic. For the TOW programs, RCA was given complete responsibility for the test logic as well as the validation of that logic.

In addition, the validation and demonstration process requirements were upgraded so as to provide an increased number of faults to be inserted and requiring 90 percent of the faults inserted to be found for individual tape acceptance. In the TOW program, we have bettered the 90 percent acceptability on all the programs and the group average is 97.1 percent. Later contracts continued these requirements and for the LCSS and TOW GO/No-Go tapes a 95 percent acceptance criteria was required.

Support Variables

At the time LCSS was conceived, the maintenance philosophy for the prime systems called for piece part replacement in the field. This support concept applied as well to the LCSS itself and presumed repair of PC boards by replacement of IC chips. This meant that diagnostic software would be needed for subassemblies down to the piece part, or in some cases, to the non-repairable module. Aside from the software, impulse soldering devices were planned for the TSM-94 Repair and Storage Van so that IC chips could be removed and replaced.

This maintenance concept has been modified to the point that conventional piece parts (transistors, capacitors, etc.) would be replaced in the field but not IC's. Also, PC boards composed primarily of IC's would not be repaired in the field. This has the effect of shifting the card repair work load to Depot level, while requiring spare card stocks at the intermediate maintenance level.

Similarly, there have been significant shifts in expected deployment of the various missile systems over the period that LCSS and the weapons were in development. These two variables, support concept and weapon deployment, point to the need for continually examining the support requirement which the test system was intended to meet and to recognize the value of flexibility in application.

COST DRIVERS

The LCSS systems, divided into the functional elements used to assess component costs, is shown in Figure 3. With some exceptions, the shaded functional elements can be matched to the costs shown in Table 1. One of the exceptions is the electro-optical bench which contains several cost components and a judgement was made in dividing the bench costs.

The test equipment cost information shown on the matrix in Table 1 is based on costs in production of sixteen systems. The sixteen systems were produced as the last run of production so that costs incorporate end-of-run learning curve recurring costs.

The categories of hardware content in the matrix, such as stimuli, measurements, etc. are indicative of the major elements of the test equipment. The data processor and the control system should be considered together, equalling 22 percent of the total system cost. The LCSS contains an electro-optical subsystem which does not quite fit the category of test equipment subsystem. The electro-optical subsystem was allocated partly to measurements and partly to enclosures/racks; the latter because of the optical bench assembly which is a precision mechanical assembly.

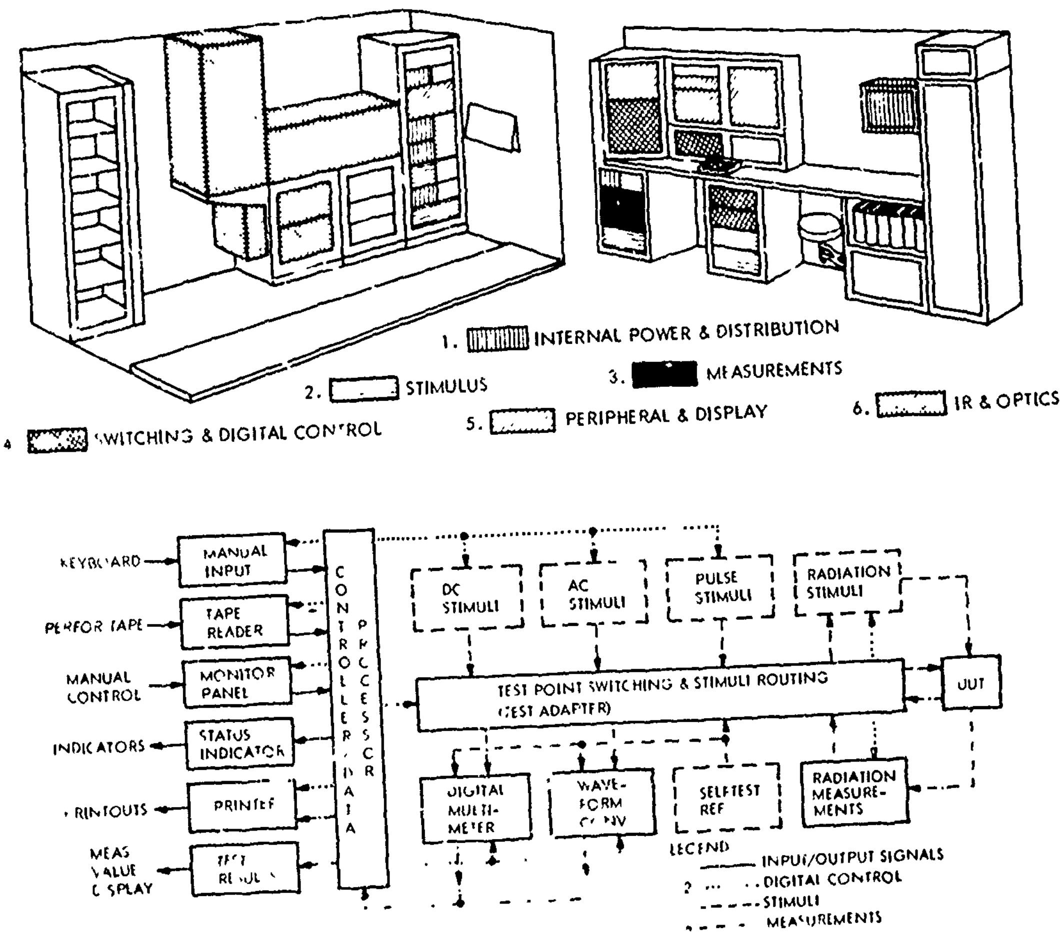

Figure 3. LCSS Functiona' Elements.

Table 1. LCSS Cost Distribution Table by Percentage

	Material	Purchased Parts	Process and Fabrication	Assembly	Test and Inspection	Support	Percent Cost Production
HARDWARE							
Stimuli Systems	52	6	24	3	9	6	17
Measurement System	55	1	21	4	12	7	10
Power System	30	20	33	2	8	7	6
Control System	33	12	39	1	8	7	20
Environmental Control System	27	18	29	6	13	7	2
Data Processor	28	-	26	17	23	6	2
Switch Network	20	8	39	7	19	7	4
Special Panel/Display	31	11	38	4	9	7	7
Cable/Harness	51	-	27	2	11	7	5
Enclosure/Racks	65	-	23	1	4	7	10
SUPPORT SOFTWARE							
Unit Under Test						100	17

From Table 1, the highest cost content comes from the stimulus, control system, and unit under test software, - each being over 15 percent. The stimulus subsystem is largely analog and reflects the requirement for accurate and stable signal generation.

The control subsystem is predominately digital. Although digital components cost per function have dropped dramatically compared to analog functions, the control subsystem is quite complex. Its role in modern automatic test system architecture is changing and this is one of the significant technological trends.

The unit under test software deserves special mention because this cost element is significant, because it is the often misunderstood, and because it is the subject of a technology proposal. Just as manual test equipment must be supplemented by a test procedure or test program to become usable, test programs are needed to supplement automatic test. The test program, like the test procedure, is unique to the prime equipment being tested. Its development is a one-time cost. The cost element shown in Table 1 as unit under test software, is the cost of test programs (both software and interface adapters) for these missile system programs which were phased in time with the build of sixteen systems.

The cost relationship between test equipment hardware and UUT software will vary with each project because this relationship is a function of:

(1) The number of test equipment sets being built, and

(2) The number of UUT test programs required.

To say simply "The software costs as much as the hardware" or "software costs are three times the hardware costs" is not adequate, although each statement may be true. It is more useful to consider hardware cost by cost elements as indicated in Table 1. It is more useful to examine software costs by a common denominator such as "cost per test" - where a test includes all the steps necessary to connect, stimulate, measure, and make a decision as to the test result. "Cost" is the total cost of the finished product, - a validated test program ready for field use.

FUTURE TRENDS

Hardware

In test equipment hardware there are two technology trends which tend to reduce cost - rather - which tend to hold costs constant in spite of increasing material and labor costs. First, more of the test equipment functions are using digital rather than analog devices. LSI and hybrid technology in test equipment application permits more logic functions per component, following a similar trend in the prime missile systems hardware. Second, the control processor subsystem is taking on more of the stimulus/measurement function. This means that it is not necessary to build hardware signal generators for each test equipment - a recurring hardware cost. This is accomplished by replicating software algorithms for the control processor. These two trends are typical of what has come to be called "third generation" automatic test equipment.

Software

On the basis of cost per test step, the trend over the past ten years is indicated in

Figure 4. The cost reduction has come from adapting production techniques in place of the model-shop environment of early UUT software developments. In the area of digital programming, the recent cost reduction has been made primarily through the use of automated test program generation (ATPG) tools. ATPG is itself a software program. ATPG, as with computer aided design, automates the test design function and does it so well that step-by-step validation of the end product is not necessary. Validation was formerly about 45 percent of the test program cost; for digital programs subject to ATPG, the cost is insignificant.

With reference to Figure 4, first generation automatic testing equipment (ATE) relied on a fixed-memory programmer-comparator to control a series of discrete devices for each stimulus generated and each parameter measured.

Second generation ATE added computer control, wideband stimulus generation and multi-function meters for measurement.

There are two ATPG problem areas which are susceptible to solution by concentrated effort supported by adequate DoD funds. The most prominent is analog test design. There has been some work in this area in the past, but the problem remains unsolved. Test design and program validation for analog devices (e.g., servo amplifiers, radio receivers) is a manual process requiring unique engineering/technician skills and generally a low initial product acceptability. Successful analog ATPG would reduce the cost per test to 20 to 40 percent of the present cost. In the second area the problem has grown faster than the tool. Most ATE manufacturers routinely use such digital ATPG tools as LASAR, D-LASAR, TESTGEN, etc. However with the trends toward large scale integrated arrays, the available ATPG are not adequate. We need more powerful simulators to handle the large scale ICs coming into use. A technology proposal for dollar saving solutions in this area follows.

TITLE: Manufacturing Technology Project to Provide a Lower Cost Process for ATE Software Production

System/Panel Area/Component: Missile System Test Equipment/ATE/Application (UUT) Software

Problem: Automated test equipment for missile system support offers advantage in testing rate and operator skill trade-offs by performing tests accurately and consistently under step-by-step control of a prepared test program. The test programs, like manual test procedures, are unique to the tested items and their preparation is a significant non-recurring cost. Depending on the number of tested items, the cost of test program preparation can be larger than the test equipment hardware costs and is often the gating item in meeting missile system operational dates.

Proposed Solution: The two primary cost drivers in test program preparation are (1) test design and (2) program validation. Validation is significant because it is necessary to verify adequate test design. Higher confidence in test design will reduce costs of validation. The test design process is amenable to computer-aided-design technology applied to fault diagnosis of missile system electronic, electro-optic, and electro-mechanical subsystems. Some progress has been made in automated program generation for digital circuits, but much remains

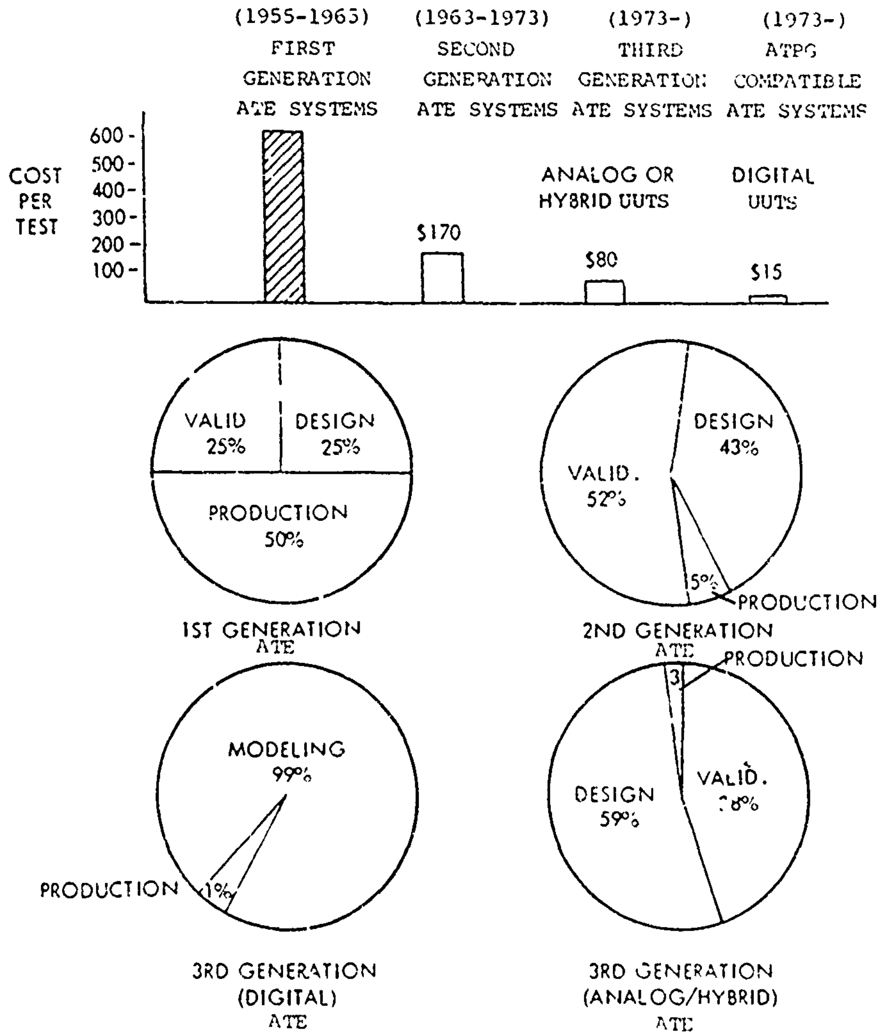

Figure 4. Test Program Set Cost Factors.

to be accomplished in test of LSI devices. Systems and circuit simulation technology should be applied to test program preparation for analog subsystems and components. Successful processes will reduce program unit costs by 40 to 60 percent in test design and 60 to 80 percent in validation.

Project Cost and Duration:

Task 1:	Extend digital ATPG to MSI, LSI	$200,000
Task 2:	Develop ATPG for analog components	$500,000
		$700,000

Estimated duration of Task 1 is twenty four months, Task 2 is thirty six months.

Benefits: The benefits to be derived are a reduction in non-recurring test program preparation costs. Cost reduction would be on the order of 60 percent for program unit costs. Typical present day costs of $50K per test program could be expected to be reduced to $20K. For a single missile system requiring 200 test programs, a savings of $6 million could be achievable with additional down-stream recurring cost savings in test program maintenance.

Assumptions: Missile system support concepts will continue to require intermediate and depot level maintenance with repair by component replacement.

MANUFACTURING TECHNOLOGY PROJECT TO REDUCE NON-RECURRING COSTS OF AUTOMATIC TESTING SOFTWARE

P. W. Shelton, Director of Engineering Product Support Services
and
M. T. Ellis, Program Manager of ATE/Test Systems

PRD Electronics

Syosset, New York

ABSTRACT

The high cost of generating Test Program Sets for the Automatic Test Equipment (ATE) that the modern complex weapons systems dictate is evident to everyone involved in the support of these systems. This paper suggests two ways of significantly reducing that cost. One approach involves the discipline and management techniques involved in the generation of the test programs themselves. The other approach involves an overall systems approach to reduce the redundancy usually incurred in generating separate and distinct test programs for the factory acceptance ATE and the field maintenance ATE stations. The complete integration of manufacturing acceptance testing with field maintenance testing will be inherent in the latter cost reduction approach.

INTRODUCTION

The complexity of modern weapons systems has reached the point where manual checkout has become unrealistic; the use of Automatic Test Equipment (ATE) with its associated high speeds and improved confidence levels is now mandatory for many systems and system components.

While the use of ATE can reduce the life-cycle support costs of the weapons systems, it brings with it an initial cost, which, to the uninitiated, may appear staggering. It is not unusual to find hardware procurement costs of several millions of dollars, and, while this is palatable for hardware which can be seen and measured by standard criteria, the software support bill, sometimes approaching $100 million for a modern military aircraft, is indeed a hard pill to swallow. This paper will examine how and where these software costs are spent, and will show how, by a methodical approach to analysis of problem areas, significant cost savings may be achieved.

THE PROBLEM

While the apparently high cost of ATE Test Program Sets (TPS's) is of almost universal concern within the support and testing community, too little has been done to systematically reduce these costs. Much attention has been focused on the test programming language. The subject of language standardization has been approached with such goals as ".... design of a test language to reduce the cost of test programs by at least an order of magnitude." This represents a very commendable goal, which has not been realized, and probably will not be realized because it ignores the nature of the problem and the actual Test Program Set cost distribution. This paper will first address the cost of TPS development by analysis of the actual TPS cost distribution.

A second problem which aggravates the cost for Test Program Sets is that there is usually a hidden cost due to redundancy. Separate and distinct TPS's are generated for the same unit under test (UUT) for factory acceptance testing and field maintenance testing. By a properly managed systems approach, the field maintenance test programs can be obtained at significant savings once the factory acceptance test programs are generated. In examining this problem it will be shown that the solution must start with the initial concept of factory acceptance and field maintenance testing.

PROPOSED SOLUTIONS

In addressing the cost of TPS generation one should never lose sight of the fact that TPS generation is a closed loop process beginning and ending with the unit under test (UUT). (See Figure 1.) The whole process begins with an analysis of the operation and system requirements of the UUT and ends with the minimum amount of testing to ensure that those requirements are adequately performed during intended usage.

The first step in proposing methods of reducing the cost of Test Program Set generation must be a more detailed analysis of the cost distribution of the effort.

Figure 2 shows a simplified flow chart of the phases of TPS development. To analyze the relative cost of each phase it is necessary to obtain quantitative data for a representative population of units under test (UUT's). From a maintenance standpoint, we can subdivide the population into two types of units: Shop Replaceable Assemblies (SRA's) and Weapon Replaceable Assemblies (WRA's). WRA's are typically the "black box" level of equipment; for example, a transceiver set. The SRA level refers to plug-in modules and subassemblies; for example, a printed circuit card. The analysis shown refers to SRA level UUT's, and specifically to printed circuit boards of both analog and digital design. The percentage of cost per phase state for black-box assembly TPS development is approximately the same as that for development of plug-in modules.

Based on a sample of approximately 300 VAST modules, with about two-thirds being digital and one-third being analog, the percentage of cost per phase state for TPS development is as follows:

		Cost (%)
1.	Test Requirement Generation	40
2.	Code - Compile	10
3.	Adapter Design and Fabrication	20
4.	Debug and Validation	20
5.	Documentation	10
	TOTAL	100

The first phase, that of Test Requirement Generation, involves the analysis of the UUT, the test environment, and the methods of testing consistent with the end test results and confidence levels. This phase will involve such things as definition of a failure, definition of fault isolation requirements and preparation of test plans, and parameter tolerances consistent with these goals. In short, this first phase lays the foundation upon which the remainder of the TPS generation task will be built. Its importance is reflected by the fact that approximately 40 percent of the total effort is expended in this phase.

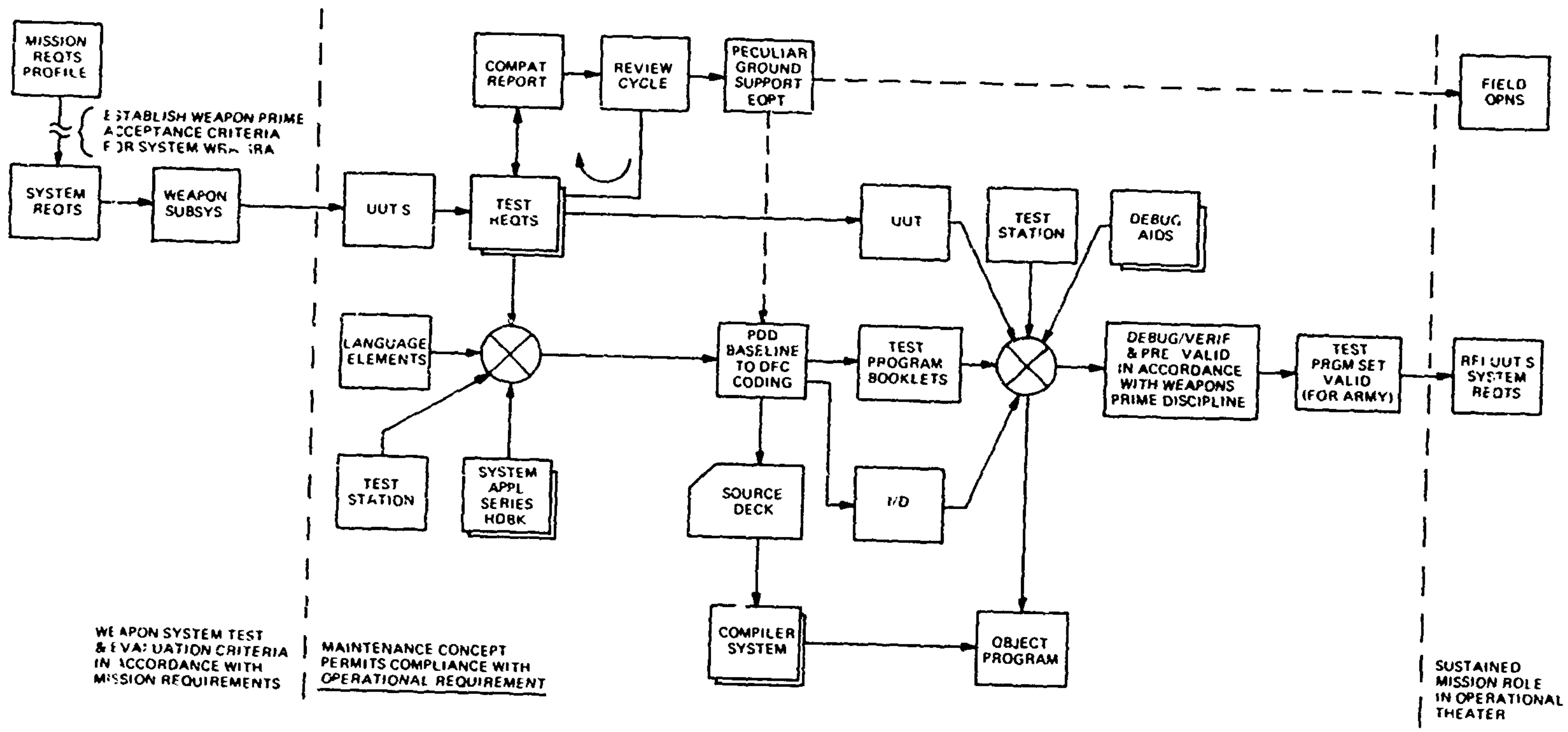

Figure 1. Closed Loop Concept for Test Program Set Development Work Flow

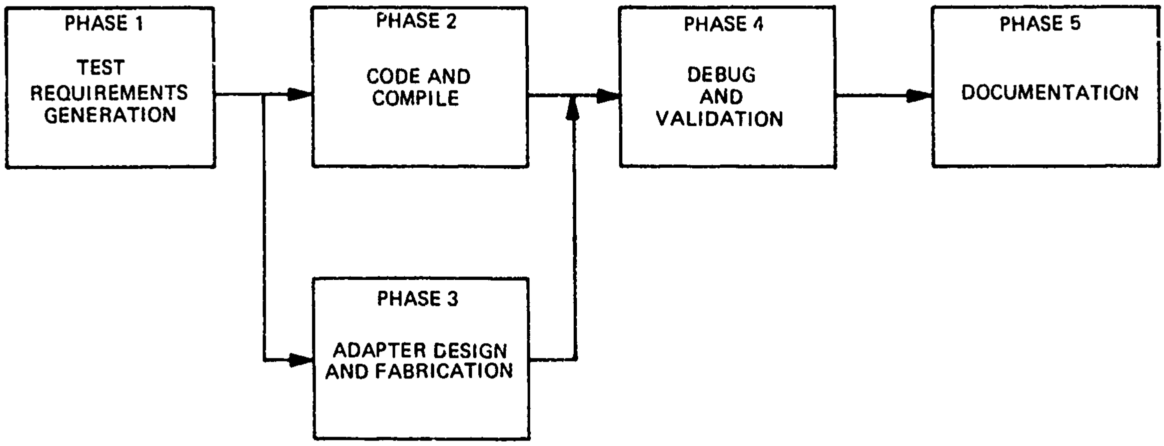

Figure 2. Test Program Generation - A Five-Phase Approach

The second phase involves the conversion of the test requirements into a form acceptable to the ATE. For most computer-controlled test systems, this is a two-step process. The first step normally consists of coding, or writing a test program in an English-like test program language. The second step consists of translating (or compiling) this program into a direct machine-executable code; in this format it is referred to as the Object Program.

For digital modules the cost of the second phase can be reduced by combining Automatic Test Generation (ATG) with a software processor to eliminate the coding effort. In this manner, the process from circuit modeling, required for ATG, to Object Program is handled by computer programs.

The third phase, design of an adapter or Interface Device, is normally done in parallel with the program coding. The Interface Device (ID) will allow the ATE to interface with the UUT. This adapter may take the form of a simple, hardwired unit designed to accommodate differences in connectors, or it may include active or passive components to provide specific signals or signal conditioning not available from the ATE. It should be noted that while the final design of the ID is done in this phase the design approach will have been determined in Phase 1. Further, the ATE design should minimize the complexity of the ID's.

The fourth phase, Debug and Validation, involves bringing together the outputs of Phases 2 and 3 and integrating these with the UUT and the ATE. While at first glance it may appear that most of the debug effort consists of correcting errors from these phases, in actual fact, most of the time (and hence money) spent in this phase is due to imperfect execution of Phase 1, the Test Requirement Generation.

The debugging in Phase 4 is concluded by some formal, previously defined validation which will demonstrate the final item quality.

The fifth phase, Documentation, is the effort necessary to:

(1) process and deliver the TPS documentation, including ATP's (Acceptance Test Procedures) and ATR's (Acceptance Test Reports), for the test program and the production version of the Interface Devices. It also includes the processing and delivery of the MIL-D-1000 drawings for the Interface Devices, the Diagnostic Flow Charts and Source Deck Listings;

(2) generate and deliver the MTPSI's (Master Test Program Set Indices), the SER's (Support Equipment Requirements), SEL's (Support Equipment Lists) and

(3) maintain configuration and documentation control, and support a documentation data bank facility.

Documentation does not include, for example, the generating of factory operation sheets, factory test procedures and deliverable drawings for ID's. These costs are included in Phase 3.

One very important factor in reducing the overall cost of TPS generation is to ensure that the effort is performed in accordance with strict discipline. It is, after all, essentially an extensive software development effort and the cost of software development is unforgiving of a lack of applied discipline. Based on experience with approximately 500 test programs over the past 5 or 6 years, PRD has developed a management/implementation plan which takes the basic five-phase approach and divides it down into 11 sub-phases with definitive review and checkpoints along the way. These checkpoints allow management to enforce the proper discipline as an on-going process rather than be confronted with a fiasco at the time that the development of a TPS was supposedly completed.

It is apparent, based on the task description and cost breakdown presented previously, that the most significant area for potential cost savings must be in the Test Requirement Generation Phase. As mentioned earlier, in addition to reducing the direct cost of that phase itself, a better quality test requirement specification will also be reflected in terms of reduced debug costs.

The following are some of the factors which, if properly taken into account during this phase, will significantly reduce the overall cost of TPS development:

- Attention should be constantly focused on the fact that the objective is "maintenance" and "factory acceptance" testing as opposed to "design verification" testing.

- Testing should be as simple as possible since this will reduce the cost of TPS development in every phase, particularly the debug phase.

- The testing of the UUT should be approached from a systems point of view; i.e., optimum utilization of the overall "system" which consists of the language, compiler, UUT and Interface Device, in addition to the test station hardware and on-station software. PRD has repeatedly demonstrated, via pilot programs, that less expensive TPS costs, shorter station run-times and less complex Interface Devices are the results of the proper "systems" approach.

- Automatic Test Generation (ATG) should be used to the maximum extent possible and, as previously mentioned, auto-coding should be employed in conjunction with ATG.

- The development of TPS's must be broken down into clearly defined phases which can be reviewed and monitored by management as an on-going process.

- Design-to-Guidelines for TPS's must be established so that the maximum of standardization that is practical is achieved by the entire work force involved in TPS's for all of the units under test of the weapons systems. This ensures that test programs for common circuits are designed only once and as a by-product assures that the debug effort is done only once.

Figure 3 summarizes the cost reduction trend that can be achieved by utilization of the foregoing techniques. The dotted curve shows the initial unit cost to the U.S. Navy

of a group of avionic Test Program Sets and the Navy's projection at that time of the theoretical decrease in cost that might be obtained based on standard learning curves. Using the initial ATE cost as a baseline, the solid curves show unit cost for PRD to develop equivalent SRA Test Program Sets for two pilot programs (F-14A and S-3A modules) and VAST Self-Test Test Programs. It should be noted that the cost for the VAST Self-Test Test Programs reflects a completely military type of contract performance with full documentation and Navy surveillance and acceptance testing of each Test Program Set. The F-14A and S-3A Pilot Programs were not formal programs nor was a complete set of documentation generated. However they serve to set cost goals that should eventually be obtained.

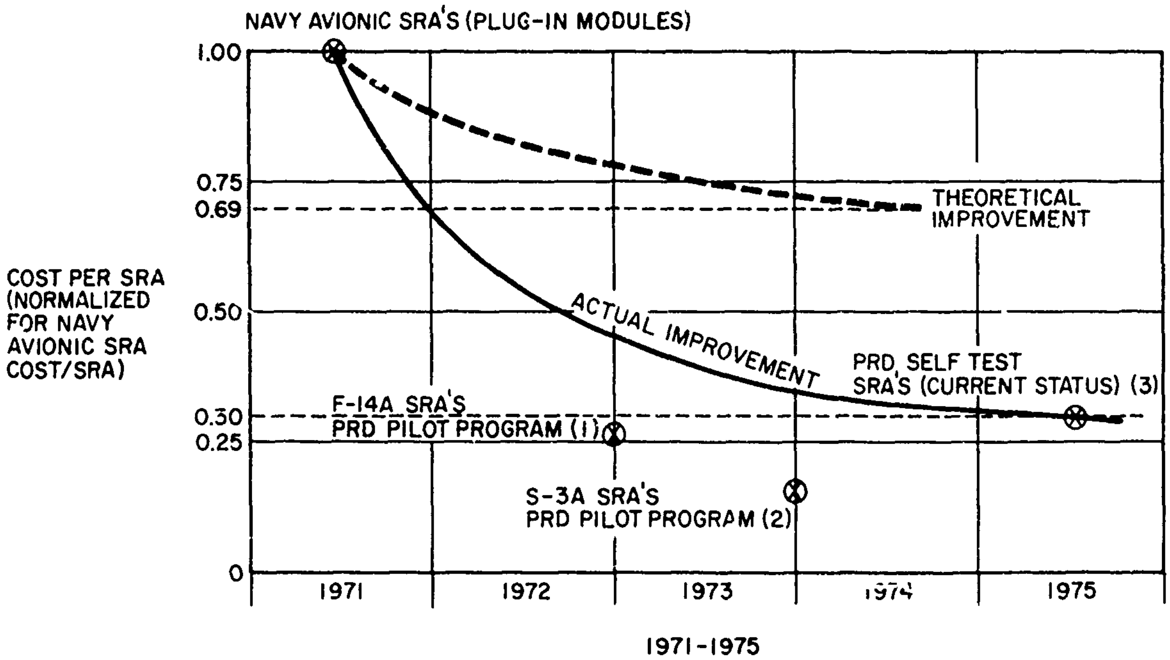

Figure 3. VAST Program TPS Cost Reduction - 1971 thru 1975

If we compare PRD's current cost per SRA Test Program Set (0.30 in a normalized basis) with the theoretical goal the Navy thought possible (0.69), it is evident that a further savings of 56 percent (0.69 - 0.30)/0.69 has been actually achieved on generation of VAST Self-Test TPS's for plug-in modules.

Assuming that the cost of the development of Test Program Sets has been minimized, life-cycle costs can be further reduced by elimination of the generation of redundant TPS's for both factory acceptance testing and field maintenance testing. To achieve this, PRD devised their "software transferability" concept. Essentially, the concept embraces the idea that the Automatic Test Equipment used for factory acceptance testing of weapon system modules can be a commercial subset (Simulator) of the militarized ATE system used for field maintenance. If this is so, the systems software (language, compiler and associated software processors) can be so designed that a source program can be processed by the software to output an object program for either the militarized ATE system or the factory ATE system, i.e., software transferability. In this manner, a TPS for a given UUT need be developed and debugged only once for either the factory ATE system or the militarized ATE system. This same source program is then recompiled yielding an Object Program for the other ATE system without incurring the cost of a completely new TPS. Figure 4 is a flow diagram of this concept, and Figure 5 is a pictorial representation of the system elements involved.

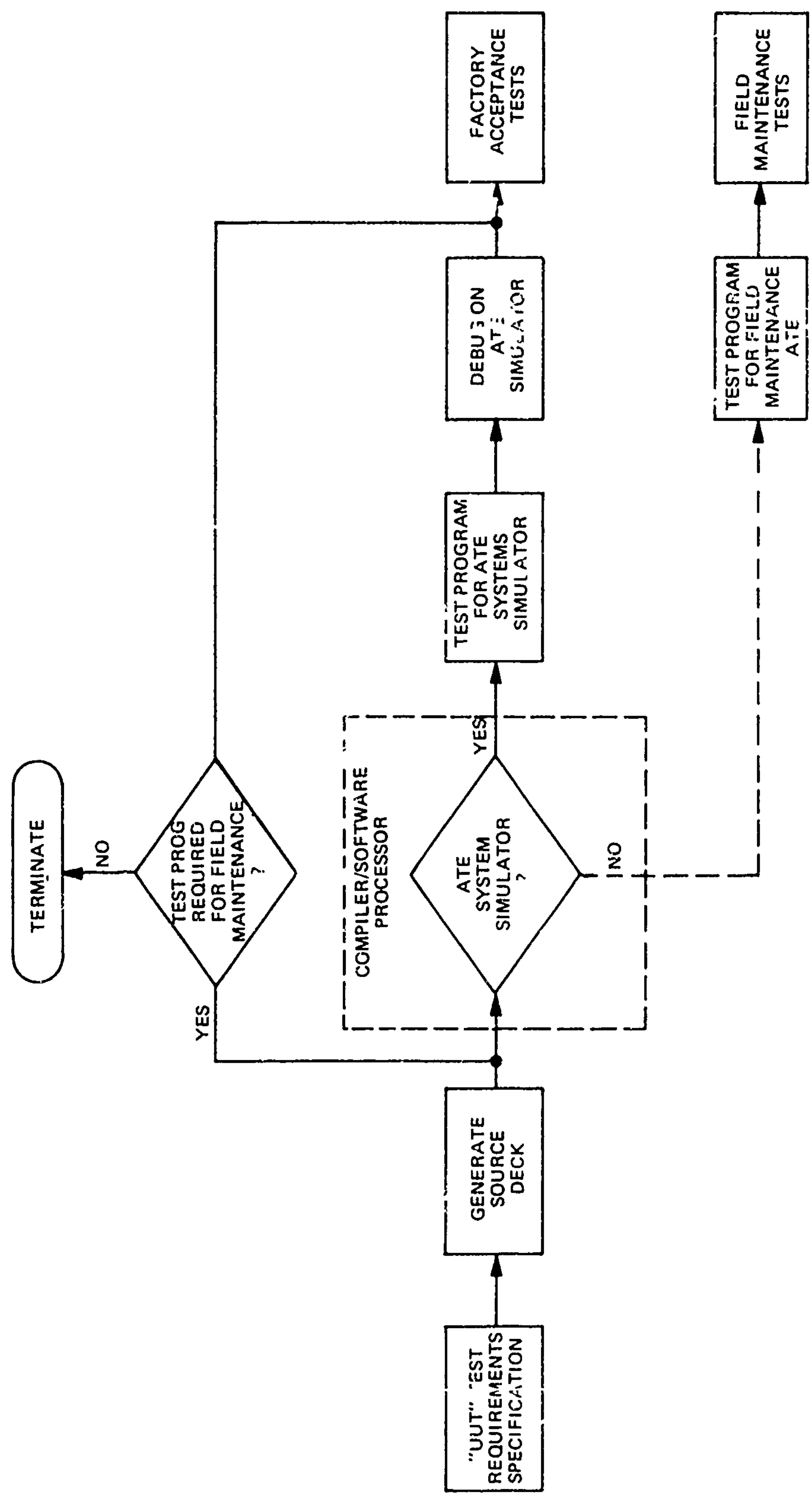

Figure 4. Flow Diagram of Software Transferability Concept

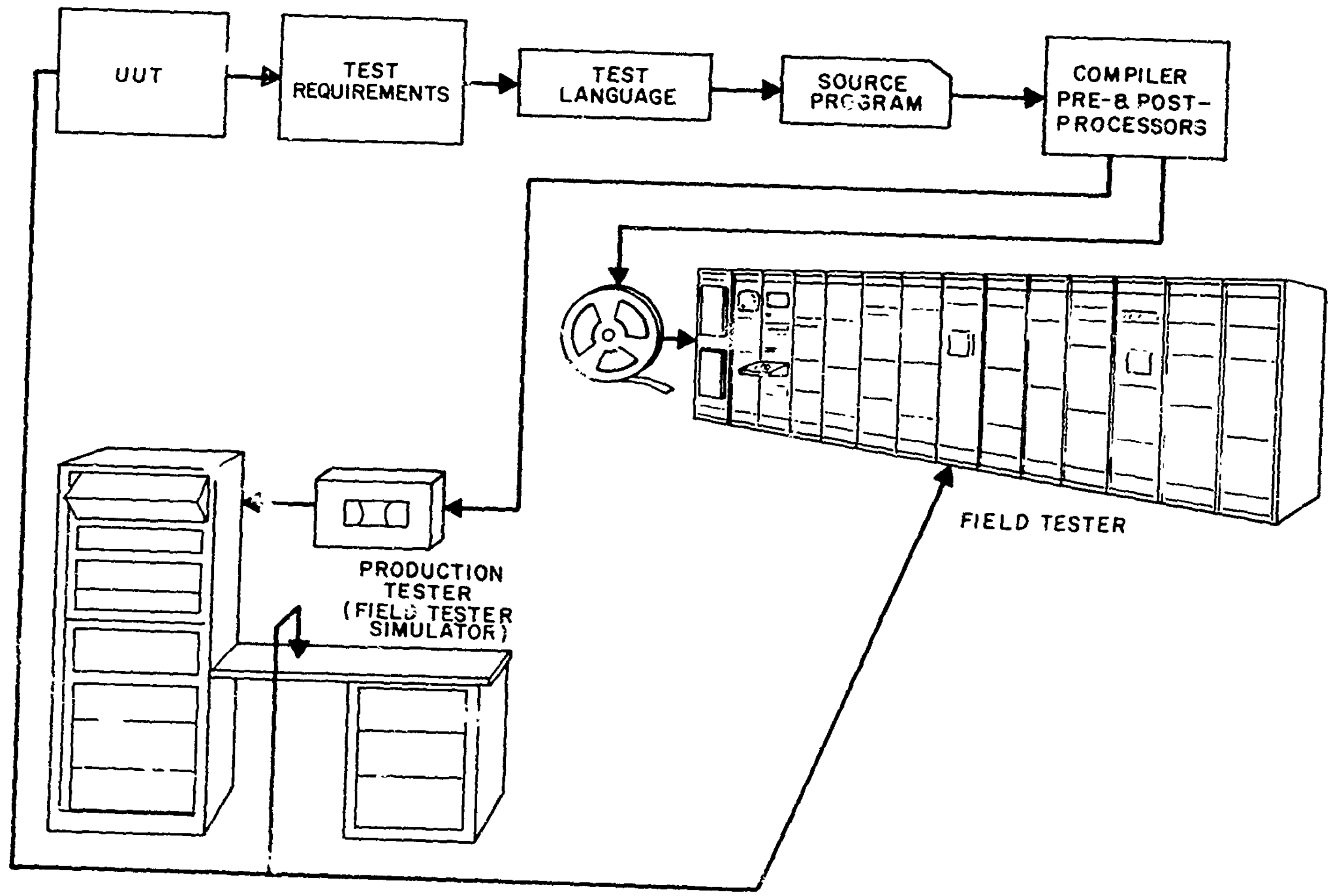

Figure 5. Software Transferability for Two Different Test Stations

PRD has been involved, over the past decade, in the development and production of VAST, AN/USM-247(V), a general-purpose militarized, automatic test system for the U.S. Navy. Inherent in the production of this test system is the development of self-test programs for each of the test system modules; thus allowing the system to, in fact, test itself. The systems in question represent a cost of approximately $2 million per station; therefore, it was mandatory that maximum use be made of each test station and, consequently, debug time in a "hands-on" mode was at a premium.

By utilization of the Simulator to debug the self-test TPS's, critical VAST station time was saved while simultaneously producing TPS's for factory acceptance testing.

The VAST station contains approximately 1,000 unique modules. Initially, a subset of 300 modules, digital in nature, was chosen and a commercial subset (VAST Simulator) factory ATE station designed which was capable of testing these modules. The concept was proven by the fact that the cost to develop a factory acceptance TPS after a self-test TPS was debugged was only 18 percent of the cost to generate a factory acceptance TPS from ground zero. The fact that the concept was proved by compiling factory ATE Simulator TPS's once field maintenance ATE Test Program Sets had been generated, instead of the reverse process, was due to the chronology of the VAST and VAST Simulator programs.

A second VAST Simulator has now been produced which has the capability of testing a subset of 700 of the 1,000 unique modules. This version is now demonstrating its utility not only in the factory but also aboard ship. Because of the software transferability concept, the Navy has the option of testing VAST modules either on VAST or the VAST Simulator while paying the cost for development of only one Test Program Set. It should be noted that the Interface Devices can be used interchangeably on the VAST or the VAST Simulator; therefore, the Navy saves the cost of procurement (and the space of storage aboard ship) of two different types of Interface Adapters.

Looking at the application of this concept in a future U.S. Army missile program, it would be expected that the factory acceptance test programs would be generated initially and the field maintenance programs derived from these. The experience on the VAST program shows that the cost of generating a field maintenance test program for a plug-in module once a factory acceptance test program is available, relative to generating a field maintenance program from ground zero, is 67 percent or a savings of 33 percent. The fact that it is not a much smaller percentage is due to the increased formality, government surveillance and acceptance, and documentation required for the field test programs as opposed to the factory test programs. The basic "engineering" effort does not have to be repeated. Let us assume that when the ground control electronic equipment and the missile electronic equipment is considered, 300 unique plug-in modules are involved. Assuming that at least one-half of them could be interchangeably tested on either the field maintenance ATE or the factory acceptance "Simulator," the cost of generating field test programs for all the plug-in modules would be reduced by 16 percent (i.e., 50% x 33% = 16%).

To implement these approaches to the reduction of the non-recurring cost of automatic testing software on future Army missile systems, or Army weapon systems in general for that matter, it is proposed that a manufacturing technology project to develop System Design Criteria be initiated. The availability of such criteria would enable the implementation of the software transferability concept and a disciplined management approach to the generation of future test programs. It is envisioned that the output of the project would be a series of reports which would define and list the specifications and constraints necessary in the areas of:

1. TPS Development
2. Language Development and/or Use
3. Compiler
4. Software Processors
5. Field Maintenance ATE Station
6. Factory Acceptance ATE Station (Simulator)
7. On-Station Software

It is estimated that the project would cost approximately $98,000 and take about 6 months.

A partial list of the projected areas to be addressed in producing such System Design Criteria is as follows:

A. Test Program Generation

1. Define the phase states and checkpoints per phase state to permit management review and control during each stage of TPS development.

2. Define the requirements of the Test Requirement Specification (TRS).

3. How do you ensure that the TRS reflects maintenance testing and not design verification testing.

4. Define source documentation to be utilized as a basis for TPS Development.

5. Guidelines for preparing test strategy.

6. What are UUT maintenance testing requirements.

7. Relationship of TPS's to weapons systems maintenance concept.

8. Relationship of overall and constituent functional operations of the UUT to the key parameters to be tested.

9. Interrelationship of UUT and SRA tolerances (maintenance error cone).

10. How the Interface Device (ID) is to be specified at the TRS level.

11. Extent to which the TRS designer should influence the adapter design.

12. ATE data required for successful TRS design.

13. How faults are defined. What constitutes a fault at the (1) maintenance and (2) factory acceptance levels.

14. Who should prepare the TRS.

15. Who should prepare the TPS.

16. What the Diagnostic Flow Chart should and should not include.

17. What the Test Diagram should and should not include.

18. Relationship of alignments/adjustments and calibration to TPS.

19. How station run-time is minimized.

20. Where should entry points be.

21. Design-to-Guidelines for TPS's to achieve maximum standardization in producing TPS's for the UUT's in the entire weapon system.

B. Software Transferability

1. Constraints on use of language elements.

2. Constraints on Software Pre-Processor.

3. Constraints in field maintenance ATE Simulator capability.

4. Constraints on on-station software.

5. Constraints in TPS generation.

SUMMARY

The area of test equipment and its usage, perhaps because of its backstage role, lacks glamour. It is probably because of this that it has, until recently, failed to receive due attention. Even now, most efforts are focused on the design of the prime equipment and its associated software. Insufficient attention has been given to the non-recurring cost of automatic testing software. This should be corrected since the cost of ATE Test Program Sets represents a significant portion of the non-recurring support budget.

The studies recommended in this paper are intended to reverse this trend and save money. The two suggested approaches taken together should save approximately 72 percent (56% + 16%) of the costs to generate TPS's for field maintenance of the plug-in modules. In addition to the cost savings, very close integration of factory acceptance and field maintenance testing is achieved.

All evidence indicates that an amount proportionate to that saved in the plug-in module area can be saved in the WRA area by a well disciplined management approach to the generation of TPS's. Test programs for military weapons presently represent investments of hundreds of millions of dollars. Future investments will also be of this magnitude. The potential for dollar savings is enormous.

The modern army is based on reduced manpower and increased technology; to remain effective its armory must receive effective maintenance. The studies proposed here are designed to provide higher quality support at lower costs: in short, to optimize the use of the constantly waning defense dollar, a goal to which we are all, industry and military, firmly committed.

ACKNOWLEDGMENTS

The authors wish to acknowledge the assistance of T. H. O'Brien, F. A. Montenes, E. E. Forster and M. B. Weber in the preparation of this paper.

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SUMMARY SHEET

Title: Manufacturing Technology Project to Reduce Non-Recurring Costs of Automatic Testing Software

System/panel area/component: General/Missile Test Equipment/Test Program

Problem: Increases in sophistication of weapon systems are dictating the use of computer-controlled Automatic Test Equipment (ATE) for effective checkout and maintenance of these systems. For complex weapon systems, the cost of test programs can approach $100 million. Despite its high cost, the actual process of Test Program Set (TPS) development has had inadequate attention in terms of standardization and management control to achieve minimum cost. Further, the separate and distinct generation of test programs for factory acceptance testing and field maintenance testing is redundant and therefore unnecessarily costly.

Proposed Solution: PRD experience on the VAST program, AN/USM-247(V), has shown that a strictly disciplined approach properly managed can reduce the cost of test programs by a factor of approximately 2. Further, if at the outset of a weapons systems program the proper systems approach is taken, the "software transferability" concept can be implemented, significantly reducing the redundancy usually incurred by developing separate and distinct test programs for factory test equipment and field maintenance testing. Implementation of the software transferability concept involves the control of the design of the system software (language, compiler, and associated software processors), field maintenance ATE and factory acceptance ATE, to enable the production of test programs for field maintenance by rerunning the same source programs through the compiler and associated software processors, once the factory acceptance testing program has been developed and debugged on the factory acceptance ATE. In other words, manufacturing acceptance testing and field maintenance testing are completely integrated.

It is proposed that a project to develop System Design Criteria be initiated which would enable the implementation of the software transferability concept and a disciplined management approach to the generation of test programs on future U.S. Army missile programs.

Projected Cost and Duration:

Estimated Cost	$98,000
Estimated Duration of Project	6 months

Benefits: By the implementation of a disciplined and effective management approach in the generation of plug-in module Test Program Sets, this project should save approximately 56 percent of the cost of generating field test programs.

By the application of the software transferability concept, an additional 16 percent should be saved in the generation of field maintenance test programs for plug-in modules.

Taken together, the overall savings in the non-recurring ATE software cost for plug-in module field maintenance test programs should be reduced by approximately 72 percent.

Assumptions: 1) The cost savings predicted for the development of TPS's can affect most future programs and many current programs. 2) The cost savings resulting from implementation of the software transferability concept will apply only to future systems.

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TITLE: Manufacturing Technology Project to Incorporate Micro-Processors into Automatic Factory Test Equipment

SYSTEM/PANEL AREA/COMPONENT

TOW, U.S.-ROLAND, HELLFIRE/Test Equipment/Data Processors

PROBLEM:

The TOW, U.S.-ROLAND and HELLFIRE are low cost, high rate missile production programs for which factory test equipment is or will be a major cost driver. Past experience in implementing test equipment for missile production programs has indicated a need for cost effective automation. Automatic test equipment implemented with micro-processors would be less expensive to implement and to support over a program life cycle than manual, hardwire controller or mini-computer controlled equipment for the following reasons:

1. Fewer test stations required

2. More flexibility for changes

3. Less production floor space required

4. More commonality in equipment design - thus reducing recurring implementation costs

5. Lower maintenance costs

6. Lower production test times

7. More accurate testing

PROPOSED SOLUTION:

This Manufacturing Technology Project will develop a test oriented, micro-processor based, modularized controller which can be built into the test systems/product interface electronics to perform those functions not being accomplished by mini-computers and hardwired controllers.

The tasks to be accomplished by this project would include formulation of modularized micro-processor based test system controller architecture and the construction and prototype testing of the controller to develop performance/cost data for use in application trade-off analysis in new automatic test system applications.

PROJECT COST AND DURATION:

Estimated costs are as follows:

1. Define classes of functions performed by test system controllers . $ 50,000

2. Determine input/output and interrupt requirements . . . 40,000

3. Develop a test oriented software environment with emphasis on "easy" interfacing of custom interfaces 60,000

4. System design of modular micro-processor based controller . . 40,000

5. Prototype and test the micro-processor based controller . . $320,000

TOTAL $510,000

Estimated project duration is 24 months.

BENEFITS:

Benefits to be derived from this project are a reduction in recurring and non-recurring test equipment implementation costs. These reductions are as follows:

1. Reduction in recurring hardware costs for Data Processors . 60%

2. Reduction in recurring hardware costs for Cables/Harnesses . 30%

NET REDUCTION OF RECURRING HARDWARE COSTS . . . 16%

3. Reduction in non-recurring test equipment implementation costs for software 40%

NET REDUCTION OF NON-RECURRING COSTS 18%

ASSUMPTIONS:

The stated benefits are based upon current production experience and as such the following assumptions apply:

1. Future missile system technologies will lend themselves to automation techniques.

2. Procurement quantities will be sufficiently large that the implementation costs of automatic test equipment can be cost effectively amortized over the production run.

COMPANY NAME

HUGHES AIRCRAFT COMPANY

PARTICIPANT'S NAME AND TITLE, ADDRESS AND TELEPHONE NUMBER

J. L. FARNSWORTH
MANAGER, PRODUCTION ENGINEERING
HUGHES AIRCRAFT COMPANY
P. O. BOX 11337
TUCSON, ARIZONA 85734

(602) 294-5311 - Extension 6861

TITLE: Manufacturing Technology Project to Develop an Automatic Fault Isolation System for Analog Circuit Assemblies

SYSTEM/PANEL AREA/COMPONENT:

TOW, U.S.-ROLAND, HELLFIRE/Test Equipment/Simulators, Data Processors, Processor Software

PROBLEM:

Automatic high rate functional testing of production analog circuit assemblies has resulted in the detection of failures, usually within minutes or seconds, which require hours to troubleshoot and repair by conventional methods. This situation has been known to tie up large quantities of production assets due to the slow, manual fault isolation and troubleshooting methods currently available.

PROPOSED SOLUTION:

This Manufacturing Technology Project would investigate and develop cost effective methods of automatic fault isolation and troubleshooting of analog circuit assemblies. This project would include an investigation of product test access, development of prototype test fixturing and investigation of automatic test equipment software fault isolation and decision making techniques.

PROJECT COST AND DURATION:

Estimated costs are as follows:

1.	Investigation and cost trade-off analysis of test point access arrangements	$ 40,000
2.	Development and prototyping of probing techniques and fixtures	100,000
3.	Development of cost effective fault isolation signal analysis technique	160,000
4.	Implementation of a prototype instrumentation and test bay	290,000
5.	Testing and cost benefit analysis of resultant methods	60,000
	TOTAL	$650,000

Estimated project duration is 28 months.

BENEFITS:

Benefits to be derived from this project are a reduction in recurring test costs in the manufacturing operation by 35%.

ASSUMPTIONS:

The stated benefits are based upon current production experience and as such the following

assumptions apply:

1. Future missile system technologies will lend themselves to automatic fault isolation techniques.

2. Procurement quantities will be sufficiently large that the implementation costs of automatic fault isolation equipment can be cost effectively amortized over the production run.

COMPANY NAME	PARTICIPANT'S NAME AND TITLE, ADDRESS AND TELEPHONE NUMBER
HUGHES AIRCRAFT COMPANY	J. L. FARNSWORTH MANAGER, PRODUCTION ENGINEERING HUGHES AIRCRAFT COMPANY P. O. BOX 11337 TUCSON, ARIZONA 85734 (602) 294-5211 - Extension 6861

TITLE: Manufacturing Technology Project to Develop a High Rate Automatic Handling and Testing System for Non-axial Lead Components

SYSTEM/PANEL AREA/COMPONENT:

TOW, HELLFIRE, U.S.-ROLAND/Test Equipment/Components

PROBLEM:

In low cost, high rate missile production programs there exists a need to test active circuit components, DIP's, OP-AMP's, transistors, etc.; 100% for removal of defective parts prior to installation into the next assembly. Sample testing is not totally adequate to catch sufficient quantities of defective parts when applied to high volume production programs. An automatic non-axial lead test system would be less costly to implement and maintain over the life of a high volume production program than the costs incurred in detecting, isolating, and replacing the defective components after installation into more complex assemblies.

PROPOSED SOLUTION:

This Manufacturing Technology Project will investigate sources of high rate non-axial lead component handling and testing equipment. This project would include the development of a system for handling, orientating, and actively testing non-axial lead components in the quantities experienced in the TOW production and those expected in the quantity production of HELLFIRE and U.S.-ROLAND systems.

The major tasks to be accomplished by this project would include the definition of a prototype test system and the pilot production usage of this system to develop maximum efficiency and cost data for use in analysis of applications for existing or future missile programs.

PROJECT COST AND DURATION:

Estimated costs are as follows:

1.	Define system requirements	$35,000
2.	Research existing non-axial lead test systems	$8,000
3.	Design and fabricate a prototype test and handling system	$130,000
4.	System evaluation and development	$10,000
5.	Cost data analysis for efficient applications	$10,000
	TOTAL	$193,000

Estimated project duration is 16 months.

BENEFITS:

Benefits to be derived from this project are a substantial reduction in the cost of testing missile assemblies, which contain non-axial lead components, and the decrease in costs required for fault isolation and replacement of faulty components. This should result in

a reduction in recurring manufacturing costs of 1% per missile.

ASSUMPTIONS:

The stated benefits are based upon current production experience and as such the following assumptions apply:

1. Future missile system technologies will lend themselves to an automated non-axial lead component test system.

2. Procurement quantities will be sufficiently large that the implementation costs of an automated non-axial lead test system can be cost effectively amortized over the production run.

3. Component test instrumentation currently available at the Tucson Manufacturing Division will be used to support this task.

COMPANY NAME	PARTICIPANT'S NAME AND TITLE, ADDRESS AND TELEPHONE NUMBER
HUGHES AIRCRAFT COMPANY	J. L. FARNSWORTH MANAGER, PRODUCTION ENGINEERING HUGHES AIRCRAFT COMPANY P. O. BOX 11337 TUCSON, ARIZONA 85734 (602) 294-5211 - Extension 6861

TITLE: Manufacturing Technology Project to Test Electronic Components at Temperature Extremes

SYSTEM/PANEL AREA/COMPONENT:

TOW, HELLFIRE, U.S.-ROLAND/Test Equipment/Components

PROBLEM:

Due to the costs associated with using conventional environmental testing techniques most electronic components are "accepted" for manufacturing use based on lot sample test results. While this statistical sampling method assures that the majority of components released to production do meet specification, it also assures that a finite quantity do not. These faulty components are only identified after assembly, either during test or in the field. The cost of detecting, isolating and correcting these component failures this late in the product life cycle is high. A cost effective high rate environmental test system for electronic components does not exist.

SOLUTION:

Develop an environmental test system which is economical to operate under high rate conditions and is capable of testing electronic components at temperature extremes. The development of this system would involve the following efforts:

1. Define the requirements of the test system and each of its elements, i.e.,test rates, component mix, measurement capabilities, temperature extremes, target operating cost.

2. Implement a prototype of the test system.

3. Pilot usage of the prototype test system to develop cost-benefit data to determine application trade-off criteria as a function of: component type, component usage, product complexity, product reliability, etc.

PROJECT COST AND DURATION:

Estimated costs are as follows:

1.	Definition of system requirements	$30,000
2.	Design and implementation of prototype test system	$125,000
3.	Testing and cost-benefit analysis of the prototype system	$15,000
	TOTAL	$170,000

Estimated project duration is 18 months.

BENEFITS:

In addition to reducing missile life cycle cost and improving field reliability the reduction in recurring missile manufacturing cost is estimated to be 1%.

ASSUMPTIONS:

The stated benefits are based upon current production experience and as such the following assumptions apply:

1. Future missile systems will have environmental and reliability requirements equal to or more stringent than current missile systems.

2. Missile electronics will be at least as complex and performance criteria as high as they are on existing missiles.

3. Component test instrumentation currently available at the Tucson Manufacturing Division will be used to support this task.

COMPANY NAME	PARTICIPANT'S NAME AND TITLE, ADDRESS AND TELEPHONE NUMBER
HUGHES AIRCRAFT COMPANY	J. L. FARNSWORTH MANAGER, PRODUCTION ENGINEERING HUGHES AIRCRAFT COMPANY P. O. BOX 11337 TUCSON, ARIZONA 85734 (602) 294-5211 - Extension 6861

TITLE: Manufacturing Technology Project to Develop Methods of Measuring Missile Weight and Center of Gravity

SYSTEMS/PANEL AREA/COMPONENT:

TOW, U.S.-ROLAND, HELLFIRE/Test Equipment/Assembly and Test

PROBLEM:

All missiles currently being manufactured at HAC Tucson and anticipated future missiles require the measurement of weight and center of gravity of the complete missile and its component subassemblies. This is usually accomplished by measuring the unit's weight and moments about its three axes, relative to some location on the missile, then dividing the moments by the weight, to determine the center of gravity location. The weight of the unit is obtained by weighing on a scale. Depending upon the accuracy requirements, two techniques are used to make the moment measurements: 1) Direct type open loop method, and 2) Null balance method (for most accurate requirements). Both methods use a single axis balance table that measures unbalance moments about one axis at a time. This requires positioning the unit on the balance table such that the moment about each axis is measured separately. The center of gravity is then calculated by manually entering the weight data and moment data into a calculator three separate times. This results in large test times and possible tester error in reading and entering the measured parameter into the calculator.

PROPOSED SOLUTION:

This study proposes the development of a two axis system that simultaneously weighs and determines the center of gravity of the unit in two axes and displays the results in a DVM or Printer.

This program activities comprise:

1. System analysis and math model

2. Precision flexure conception and development

3. Displacement transducer selection and evaluation

4. Computation system

   a. Analog - if one measurement per axis is required

   b. Micro-processor - if multiple measurement averaging is required

5. Error analysis

6. Breadboard and evaluation

PROJECT COST AND DURATION:

Estimated costs are:

1. System Analysis and Math Model $17,000

2. Precision flexure conception and development $8,000

3. Displacement transducer selection and evaluation		$5,000
4. Computation system		$25,000
5. Error analysis		$7,500
6. Breadboard and evaluation		$24,000
	TOTAL	$86,500

Estimated project duration is 12 months.

BENEFITS:

Benefits to be derived from this project are:

1. Reduction in total missile test time — 45%
2. Reduction in possible tester error

ASSUMPTIONS:

The benefits as stated are based upon past production experience and time study analysis of existing systems, and are justified if the current trend in Weight and Center of Gravity measurements requirements continue as anticipated.

COMPANY NAME

HUGHES AIRCRAFT COMPANY

PARTICIPANT'S NAME AND TITLE, ADDRESS AND TELEPHONE NUMBER

J. L. FARNSWORTH
MANAGER, PRODUCTION ENGINEERING
HUGHES AIRCRAFT COMPANY
P. O. BOX 11337
TUCSON, ARIZONA 85734

(602) 294-5211 - Extension 6861

TITLE: Manufacturing Technology Project to Develop Accurate Methods of Measuring Medium Range Leak Rates

SYSTEMS/PANEL AREA/COMPONENT:

TOW, U.S.-ROLAND, HELLFIRE/Test Equipment/Assembly and Test

PROBLEM:

Leak rates ranging from 10^{-1} to 10^{-4} cc/sec are difficult to measure with any conventional leak test equipment. This problem becomes more difficult when these leak rates must be measured under high rate production conditions.

The Δ P test method can be utilized for leak testing but has inherent problems. The test time is inversely proportional to the magnitude of the leak, resulting in excessive test times for small leaks. Slight temperature changes cause pressure fluctuations resulting in instabilities.

The mass spectrometer test method is an accurate method for measuring small leaks from 10^{-5} to 10^{-11} cc/sec. It must operate in a vacuum environment with the most common test gas being helium. Some materials outgas when placed in a vacuum resulting in excessive pump down time that could damage the product. Helium gas permeates certain materials used in missiles and is, therefore, limited in its utilization.

The electron capture detector has proven to be an effective instrument for qualitative measurement of SF_6. It has drawbacks in quantitative measurement due to the heaviness of SF_6 and the difficulty of obtaining a homogeneous sample of test gas.

PROPOSED SOLUTION:

It is the intent of this proposal to investigate and determine the optimum method of testing for leaks of this magnitude. Automatic sampling to reduce volume, use of orifices to control conductance, and proper vacuum level to control outgassing could be incorporated with a mass spectrometer tube to measure leak rates as large as desired. Vacuum equipment such as thermocouples or ionization gauge tubes could be used to measure low pressure changes since temperature effects are minimal in a vacuum. If helium is not acceptable as a test gas, a spectrometer tube can be modified to measure another gas compatible with the product such as argon, neon, etc.

A Δ P system could be designed that would work in a vacuum by using equipment mentioned above minimizing the thermal expansion and conductivity.

The electron capture detector could be incorporated into a system that would perform quantitative measurements by sampling. A chamber capable of mixing the trace gas and background would be required.

The program would require procurement of detection components, pumps, valves controllers, vacuum gauge tubes, raw materials, and miscellaneous materials. The program activities would comprise:

1. Conceptual analysis

2. Components selection

3. Error analysis

4. Test plan

5. Breadboard and evaluation

PROJECT COST AND DURATION:

Estimated costs are:

1. Conceptual analyis		$20,000
2. Components selection		$55,000
3. Error analysis		$8,000
4. Test plan		$11,000
5. Breadboard and evaluation		$30,000
	TOTAL	$124,000

Estimated project duration is 18 months.

BENEFITS:

Benefits to be derived from this program are:

1. Achieved accuracy requirements

2. Reduced total assembly test time by as much as 40%

ASSUMPTIONS:

Justification of this program assumes, continued storage of missiles in the present conditions, the design of the subassemblies interfaces remaining unchanged and the leak rate requirements continuing in the ranges of current products.

COMPANY NAME

HUGHES AIRCRAFT COMPANY

PARTICIPANT'S NAME AND TITLE, ADDRESS AND TELEPHONE NUMBER

J. L. FARNSWORTH
MANAGER, PRODUCTION ENGINEERING
HUGHES AIRCRAFT COMPANY
P. O. BOX 11337
TUCSON, ARIZONA 85734

(602) 294-5211 - Extension 6861

Title: Manufacturing Technology Project to demonstrate the usefulness and advantages of pattern recognition as a viable technology for automatic inspection.

System/Panel Area/Component: Test Equipment - mechanical parts and electronic assemblies manufactured in large quantities.

Problem: Considerable costs are incurred in the inspection of critical parts and electronic assemblies which are used in large quantities. In addition to the high labor content in an operation of this type, the chance of human error because the repetitive nature of the work is high, a fact which can have very serious consequences. Qualified inspectors are scarce during emergency or wartime conditions.

Proposed Solution: An automatic inspection device using the principles of pattern recognition reduces inspection costs and the chance of human error. It is proposed that a system be designed and built, programmable for inspecting different configurations of missile parts to demonstrate the feasibility of the application of pattern recognition as an inspection tool. Commercially available components would be used wherever feasible.

Project Cost and Duration: Estimated costs are as follows:

Design and construction of system	$225,000
Evaluation and demonstration of system	$ 75,000
Total	$300,000

Estimated duration of the project is 24 months.

Benefits: Two extremely important benefits would be derived from this project ...
substantial reduction in labor content of parts inspection
virtual elimination of human error in inspection cycle.

Assumptions: The major suppliers of missiles and spare parts can be convinced of the economic advantages derived from the use of the inspection system.

COMPANY NAME

Westinghouse Electric Corp.

PARTICIPANT'S NAME, ADDRESS AND PHONE

J. C. McVickers, Director
Production Technology
Pittsburgh, PA. 15235
412-256-7456

Alternate
F. J. Michel, Manager
Special Projects
Production Technology
Pittsburgh, PA 15235
412-256-3548

INVESTIGATION OF INTERFACE TEST ADAPTER FOR MULTILAYER CIRCUIT BOARDS

James O'Brien

The Boeing Company

Seattle, Washington 98124

SYSTEM/SESSION AREA/COMPONENT

All Systems/Test Equipment/Printed Circuit Boards

PROBLEM

It is necessary to perform in-process continuity, insulation resistance, and dielectric strength tests on bare printed circuit boards prior to assembly of component electronics. At present, this requires the design and fabrication of a special test adapter for each board configuration. This is a non-recurring manufacturing cost which becomes rapidly more significant with decreasing test quantities.

PROPOSED SOLUTION

A universal adapter would seem to be the ideal solution; one which, with minimum time and effort, could be adapted to fit any board configuration. However, there are many problems to this approach which require investigation before it can be said that this is a feasible solution.

A most cost-effective solution may be to streamline the present design and development of special test adapters. Present technology exists in the computer aided design and computer aided manufacturing fields which might well be adapted to this purpose.

The purpose of this project would be to investigate these alternatives and develop a working prototype of the most pratical one.

PROJECT COST AND DURATION

Engineering Effort	$50,000
Materials	3,000
TOTAL	$53,000

Estimated duration of the project is 12 months.

BENEFITS

Our current interface adapters cost between $2,000 and $4,000. In addition, we expend another $3,000 to $4,000 to generate a test program. All the interfacing data required to design an adapter and to prepare a test program is in our computer aided design data base. It is possible to develop a test adapter concept and a software package which could save $4,000 to $7,000 for each multilayer board type.

EVALUATION OF CABLE TESTING METHODS

James O'Brien

The Boeing Company

Seattle, Washington 98124

SYSTEM/SESSION AREA/COMPONENT

All Systems/Test Equipment/Wire, Cables, and Harnesses

PROBLEM

There is much controversy concerning the testing of wires, cables, and harnesses. The problem areas concern what test methods are really necessary to detect faults and could present test methods cause dielectric degradation under certain conditions. The limits of testing and the results of overtesting need to be delineated.

PROPOSED SOLUTION

A review would be made of all applicable literature on the subject. Manufacturers of wire and cable and of military products will be contacted. The review will result in a report which will summarize the current state-of-the-art in cable testing. It would recommend improved methods or point out areas where present knowledge is lacking and in need of further research.

PROJECT COST AND DURATION

Data Collection and Evaluation	$12,000
Report Preparation	4,000
TOTAL	$16,000

The duration of the study would be four months.

BENEFITS

Present Level I testing (go-no-go continuity, short circuit, insulation resistance) takes approximately 1.2 hours for a typical 1000 path circuit. Increasing the test complexity to Level 2 (continuity with measured resitance values, dielectric withstand, insulation resistance, capacitance, and VSWR) increases the test time for the same circuit to approximately eight hours.

Since it is not always clearly understood just how much testing is required to prove a circuit, it is probable that many circuits are overtested just to be "sure". As can be seen from the "typical" circuit example, any extra testing adds significantly to test time and cost. A better definition of cable testing methods and requirements would help to avoid the high costs of overtesting.

AUTOMATIC ADAPTIVE CONTROL PRINTED
WIRING BOARD PLATING SYSTEM

R. R. Schulze

Hughes Aircraft Company
Fullerton, California 92634

SYSTEM/PANEL AREA/COMPONENT

Various/Test Equipment/Printed Circuits.

PROBLEM

Many variable parameters are involved in the electro-plating of PWBs, e.g., solution type, purity, temperature and contaminants; plating current density; PWB pattern density and distribution; cleaning solutions and rinses; time in solution; time out of solution; etc. To maintain overall quality of the finished PWB, very tight tolerances must be maintained on each parameter. If a parameter drifts or ages, the entire process must stop until that parameter is brought back into tolerance, or some other parameter(s) must be changed to compensate.

Secondly, since plating sequences vary between part numbers and/or customers, the small lot production facility must "re-tune" each time a different part type is processed.

PROPOSED SOLUTION

A computerized system which monitors and controls the many parameters of the total plating operation. It must be adaptive, i.e., it must be capable of controlling one or more parameters to compensate for drift or variance in other parameters.

The principle effort is the development of an algorithm, programmed and executed in an inexpensive local minicomputer.

PROJECT COST AND DURATION

Estimated costs are:

Design, Code and Testing	$250,000
Pilot Implementation	150,000
Total	$400,000

Duration of this project is estimated at 24 months.

BENEFITS

Benefits to be derived from the successful completion of this project are:

- Better quality PWBs.
- Lower PWB costs by reducing labor and scrap.
- Increased productivity.
- Can be implemented in large or small shops alike.

ASSUMPTIONS

The stated benefits assume the availability of in-tank sensors and controls for detecting and maintaining plating parameters.

If the plating operation is to be completely automatic, it also assumes a robot or material handling system.

HEAT PIPES IN HIGH POWER SEMICONDUCTOR DEVICES

Dr. K. S. Sekhon

Hughes Aircraft Company
Fullerton, California 92634

SYSTEM/PANEL AREA/COMPONENT

Various/Test Equipment/Environmental Control.

PROBLEM

Advances in semiconductor technology have opened the way for higher speed circuits and higher component density, resulting in higher temperatures which adversely affect the switching time, frequency response and reliability of the device. These thermal considerations are limiting the application of further developments in semiconductor technology. Heat pipes, which use an evaporation-condensation cycle of a fluid powered by capillary forces to transfer thermal energy, provide an alternative method for cooling high power density devices by direct cooling of the semiconductor chip. Hughes-Fullerton has developed such a heat pipe for use in cooling power transistors. In a study for the United States Army Electronics Command (Contract DAAB07-72-C-0021) Hughes located heat pipes directly on the chips of 2N5701 transistors operating at 76 MHz. The heat pipe dramatically lowered the operating junction temperature as the report fully documents. Test data shows that the thermal resistance was cut by 80%. A significant increase in chip reliability results from decreased temperature. The heat pipe cooling technique is not limited to megaHertz devices, but can be extended to gigaHertz devices with still smaller chips. The major problem with the incorporation of a heat pipe into a high power semiconductor is the cost. The manufacturing costs have to be reduced significantly to make use of the already developed heat pipe technology.

PROPOSED SOLUTION

The purpose of this project will be to establish cost effective production techniques for the manufacture of heat pipes integral to semiconductor devices. Primary emphasis will be placed on the following items:

- Establish manufacturing techniques for wick attachment, shell fabrication and shell bonding.
- Establish a vacuum/fill station for high volume production.
- Establish a test station for thermal and dynamic performance verification.
- Procure necessary equipment for production procedures.

- Execution of a typical production run for verification of quantity production techniques.

This project will reduce the cost of manufacturing heat pipes for semiconductors from $750 per device to $35 per device.

PROJECT COST AND DURATION

Pilot Equipment Design	$85,000
Pilot Equipment Fabrication	55,000
Pilot Equipment Installation	10,000
Pilot Production and Technical Data	15,000
Total	$165,000

Estimated duration of the project is 12 months.

BENEFITS

Benefits to be derived from project are a reduction in recurring costs to incorporate heat pipes in high power semiconductors. It is anticipated that this project will reduce the manufacturing costs from $750 to $35 per device. Furthermore, it will:

- Make available techniques, procedures and data for the quantity production of high thermal efficiency semiconductors utilizing internal heat pipes.

- Establish manufacturing methods and data to meet the requirements of high power density R.F. semiconductors used in current and future electronic systems. The application of heat pipes to semiconductor devices is not limited to one type of chip or package configuration, but can be used for any sealed package device provided that the wick and fluid are chemically and electrically compatible with the semiconductor.

- Result in a significant increase in production rates and cost reduction.

ASSUMPTIONS

The stated benefits assume that a heat pipe/semiconductor production facility will be set up and optimized. It also is assumed that production rate would be 250 devices/month.

CONTROL PARAMETERS FOR THE TIN/LEAD
PLATING AND FUSING OF PRINTED WIRING BOARDS

J. R. Kubik

HUGHES AIRCRAFT COMPANY
Fullerton, California 92634

SYSTEM/PANEL AREA/COMPONENT

Various/Test Equipment/Printed Circuits.

PROBLEM

Parameters and techniques for plating and fusing of tin/lead coated printed wiring boards (PWBs) are not currently established per military documentation which results in low yield production and less reliable electronic assemblies.

The quality of any tin-lead deposit is dependent on many factors, e.g., a receptive clean metallic substrate, plating bath control, purity of anodes, bath impurity control, micro and macro throwing power, optimization of alloy composition and brightener content. Improper control of these factors results in poor solderability, etching difficulties, dewetting, and contamination, all of which impose problems in subsequent testing and production operations.

Current tin-lead fusing of PWBs is accomplished by either hot oil or glycol type liquids, hot air knife or infra-red processes. Each method has advantages and detrimental aspects which require evaluation. These variations in the heating techniques can also affect the solderability and wettability of PWBs which in turn can necessitate the usage of more active fluxes. Post fusing cleaning techniques become very important to assure freedom from contamination.

PROPOSED SOLUTION

A program to investigate and establish limitations for process variables in both tin/lead plating and fusing would alleviate many of the production yield and subsequent field problems associated with PWBs. The work description for such a program is outlined below:

Tin Lead Plating

- Establish optimum copper surface preparation parameters for Sn/Pb receptivity.
- Identify optimum plating bath criteria (solution, anode, current density, etc.) correlated to SEM and metallurgical data.
- Evaluate maximum impurity levels of foreign ions (metallic and organic) in plating bath.

- Establish criteria for Sn/Pb plating bath maintenance (testing, carbon and flow current treatment, etc.).
- Relate all development to solderability of plated Sn/Pb.
- Provide data for military and guideline documentation.

Tin Lead Fusing

- Evaluate current fusing processes (oil, hot knife, IR, etc.) in regard to PWB types, effect on the PWB, solder sag, metallurgical aspects and solderability.
- Evaluate effectivity and contaminate effect of various fluxes used for fusing processes.
- Ascertain value, attributes and detriments of Sn/Pb preconditioners.
- Establish optimum procedures and criteria for post fusing cleaning of PWBs.
- Supply data for military documentation.

PROJECT COST AND DURATION

Estimated costs are as follows:

Tin lead plating	$100,000.00
Tin lead fusing	90,000.00
Total	$190,000.00

Estimated duration of the project is 24 months.

BENEFITS

Benefits to be derived from this project include (a) the standardization of critical manufacturing methods and criteria for PWB fabrication, (b) improved reliability, (c) less rework, (d) higher production yield and (e) low production cost.

An example of savings for various systems is shown below, based on a 5% reduction in manufacturing costs. The figures utilized are considered conservative for each system (i.e., lower production rate and low average board costs).

SYSTEM	SYS/YR	PCB SAVINGS	MLB SAVINGS	TOTAL SAVINGS
PERSHING	36	$ 20,925	$ 3,870	$ 24,795
DRAGON	6000	99,000	22,500	121,500
STINGER	9000	121,500	22,500	144,000
TOW	6000	99,000	15,000	114,000
ATI	120	15,300	2,850	18,150
CHAPARRAL	3000	63,000	11,250	74,250
				$496,695

Further savings would be realized if applied to other missile systems.

ASSUMPTIONS

A 5% reduction is assumed based on the average amount of labor and material costs utilized in rework on rejection of boards due to improper solder.

PRODUCTION CLEANLINESS CRITERIA AND PROCESSES FOR PRINTED WIRING BOARDS AND ASSEMBLIES

J. R. Kubik

Hughes Aircraft Company
Fullerton, California 92634

SYSTEM/PANEL AREA/COMPONENT

Various/Test Equipment/Printed Circuits.

PROBLEM

Currently the military, through the proposed MIL-P-XXXXX printed wiring board assembly (PWBA) specification, has imposed a cleanliness requirement prior to conformal coating. This document, to be released shortly by DESC, allows the use of rosin activated (RA) type fluxes on the condition that a solvent extract of the assembly meets an ionic resistivity value of no less that two million ohm-cm. The test method described is a procedure devised by Bell Laboratories and modified by the Naval Avionics Facility, Indianapolis (NAFI). The method has merit, but is not oriented to production use where the frequency of testing necessitates simplicity and speed.

PROPOSED SOLUTION

The scope of this program will be to establish production cleanliness criteria and processes for PWBs and PWBAs.

The projected NAFI resistivity value was based on idealistically sized PWBs (not PWBAs) representing an optimum size of ten square inches of surface with very little reliability data correlatable to a maximum ionic content that would degrade the electrical performance of the PWB. Only a cursory investigation was instituted on the solvent cleaning systems to remove contaminants, ions and soils from the system.

PROJECT COST AND DURATION

Estimated costs are as follows:

Materials	$ 25,000.00
Engineering Support and Technical Data	120,000.00
Total	$145,000.00

Estimated duration of the project is 24 months.

BENEFITS

The documentation resulting from this effort will relate to increase in reliability of the PWBA and assembly service life. The net value will result in overall cost savings by decreasing failure analysis, lowering replacement costs and reducing the quantity of spare units. The cost saving resulting from these reductions is as follows:

- Reduction in failure analysis: 1% of printed wiring board cost
- Reduction in replacement cost: 2% of printed wiring board cost
- Reduction in spare units: 2% of printed wiring board cost
- Total: 5% of printed wiring board cost

An example of cost savings for specific missile systems is given below. The figures utilized are conservative (i.e., the lower production rates and low average printed wiring board costs are used).

SYSTEM	SYS/YR	PCB SAVINGS	MLB SAVINGS	TOTAL SAVINGS
PERSHING	36	$ 20,925	$ 3,870	$ 24,795
DRAGON	6000	99,000	22,500	121,500
STINGER	9000	121,500	22,500	144,000
TOW	6000	99,000	15,000	114,000
ATI	120	15,300	2,850	18,150
CHAPARRAL	3000	63,000	11,250	74,250
				$496,695

Further savings will be realized if applied to other missile systems.

ASSUMPTIONS

It is assumed that successful completion and application of information gained from an MMT program will result in a cost savings of 5% in printed wiring board fabrication by reducing the need for failure analyses, replacement costs and spare units during fabrication.

PRODUCTION CONTROL PROCESSES TO PREVENT PLATED-THROUGH-HOLE CRACKING IN PRINTED WIRING BOARDS DUE TO "Z" AXIS EXPANSION

R. W. Korb

Hughes Aircraft Company
Fullerton, California 92634

SYSTEM/PANEL AREA/COMPONENT

Various/Test Equipment/Printed Circuits.

PROBLEM

The cracking of plated-through holes as a result of z-axis expansion is a significant failure mode in multilayer printed wiring boards. This type of cracking is due to the differential expansion characteristics of epoxy glass laminates and copper plating. It is normally observed after the solder fusing or reflow operation where the board has been exposed to a temperature of 400 - 500°F.

Multilayer printed wiring boards supplied to MIL-P-55640 require thermal stress testing which prohibits any evidence of fractures of the copper plated holes after a ten second solder float test in solder maintained at 550°F (288°C). At the present time many military contractors are experiencing considerable difficulty and inconsistency in meeting this requirement.

PROPOSED SOLUTION

Although the causes of plated-through-hole cracking appear to be well understood, the remedy, i.e., to achieve sufficient ductility of the copper in the plated-through-hole, has not been established. Although there are several factors involved, ductility is basically dependent upon the plating system, operating conditions and additives.

This project will develop, evaluate and establish the optimum manufacturing processes and techniques required to plate multilayer circuit boards capable of consistently meeting the thermal stress requirement of MIL-P-55640.

PROJECT COST AND DURATION

Estimated costs are as follows:

Analytical testing	$29,000.00
Engineering manpower	91,000.00
Total	$120,000.00

Estimated duration is 24 months.

BENEFITS

Benefit to be derived from this project is a reduction in recurring hardware costs. This reduction is as follows:

Reduction in reject boards: 13% of printed circuit board cost.

An example of cost savings for specific programs is shown below. Figures utilized were lower production rates and low MLB manufacturing costs. This can be considered conservative.

SYSTEM	SYS/YR	MLB SAVINGS
PERSHING	36	$ 10,062
DRAGON	6000	58,500
STINGER	9000	58,500
TOW	6000	39,000
ATI	120	7,410
CHAPARRAL	3000	29,250
		$202,722

Further savings can be realized if applied to other missile systems.

ASSUMPTIONS

Currently, PTH cracking is one of the factors causing high rejects on MLBs. It is assumed that a considerable reduction (13%) in rejects will occur with successful completion of this program.

OPTIMIZED SOLDERING TECHNIQUES FOR PRINTED WIRING BOARDS AND ASSEMBLIES

J. R. Kubik

Hughes Aircraft Company
Fullerton, California 92634

SYSTEM/PANEL AREA/COMPONENT

Various/Test Equipment/Printed Circuits.

PROBLEM

The soldering of components to printed wiring boards (PWBs) continues to be a problem in the fabrication of highly reliable printed wiring board assemblies (PWBAs). Due to the requirements invoked and certain limitations imposed on the process, high production costs are incurred due, in many cases, to rework. Two factors greatly affecting the fabrication and assembly of PCBs are (1) the flux used and subsequent cleaning and (2) the component lead solderability. Presently, the use of RA fluxes is not permitted by military specification, however, RMA fluxes (which are permitted) do not always provide adequate cleansing action, thus affecting solderability. On the other hand, using an RA flux can result in corrosion during service if the assemblies are not cleaned adequately subsequent to soldering. An added variable is the difference in component lead solderability. Certain leads require special pre-tinning prior to a given solder assembly process, thus adding cost to the program.

PROPOSED SOLUTION

The project would provide a study of the two primary problem areas, (1) a study of corrosion effects of fluxes on PWBAs and (2) a study covering the standardization of component lead materials. By performing a controlled study of the corrosion effect from various classes of fluxes, the procedure for post flux cleaning can be established to provide highly reliable boards and assemblies. The study would also delineate specific cleaning procedures for the various fluxes. Concurrently, the study to cover standardization of component lead materials would also alleviate the need for various fluxes.

PROJECT COST AND DURATION

Estimated costs are as follows:

Corrosion effects of fluxes	\$125,000.00
Standardization of component leads	75,000.00
Total	\$200,000.00

Estimated duration of project is 24 months.

BENEFITS

Benefits derived from this project are a reduction in fabrication costs for PWBAs in all military systems using soldered PWBs and PWBAs.

It is anticipated 2% of assembly costs will be saved. An example of cost savings for specific missile systems is shown below.

SYSTEM	SYS/YR	ASSEMBLY SAVINGS
Pershing	36	$123,984.00
Dragon	6,000	600,000.00
Stinger	9,000	720,000.00
TOW	6,000	576,000.00
ATI	120	90,720.00
Chaparral	3,000	372,000.00
		$2,482,704.00

Additional cost savings will be realized if applied to other systems.

ASSUMPTIONS

It is assumed that successful completion of this program will reduce rejection rates and rework costs of PWBAs by 2% of total cost.

PRODUCTION PROCESS FOR REMOVING EPOXY SMEAR IN PLATED THROUGH HOLES (PTHs)

R. W. Korb

Hughes Aircraft Company
Fullerton, California 92634

SYSTEM/PANEL AREA/COMPONENT

Various/Test Equipment/Printed Circuits.

PROBLEM

A major cost factor in producing high reliability printed wiring boards is the removal of epoxy smear prior to plating the through holes. The most efficient present method is vapor honing using specially designed machines. Present equipment, however, is limited by hole diameter to board thickness ratio. Consequently its effectiveness is reduced in high density boards used in missile systems. Also the process causes an elongation of the boards which creates registration problems in high density close tolerance circuits. Typical board growth on a machine specifically designed for printed wiring boards is 0.008 inch over a 20 inch length on the first pass. This distance increases to 0.010 inch on the second pass, 0.011 on the third and 0.012 on the fourth pass.

Present vapor honing machines are also partially dependent on close controls in drilling and chemical cleaning which adds to the cost.

PROPOSED SOLUTION

Hughes-Fullerton, Ground Systems Group, has designed, built and tested a vapor honing machine that directs an abrasive slurry through the holes without damaging the external copper layers. As a result, processing times can be extended to enable heavy smear removal without reliance on chemical cleaning or close controls on drilling. Processing does not cause any significant elongation of the printed wiring board as found in conventional equipment. Initial measurements show a growth of only 0.0005 inch over an 18 inch length. At the present time only a prototype model of the machine has been built. This machine is too slow for production use, however, the initial results are excellent. It has demonstrated that forceful passage of an abrasive slurry through the holes effectively removes epoxy smear. Further effort is required, however to increase the speed and efficiency of the machine.

PROJECT COST AND DURATION

Estimated costs are as follows:

Machine design	$ 50,000.00
Machine fabrication	60,000.00
Pilot operation and optimization	50,000.00
Engineering support and technical data	50,000.00
Total	$210,000.00

The duration of this project is estimated to be 24 months.

BENEFITS

Benefit to be derived from this project is a reduction in manufacturing cost for high density printed wiring boards. This reduction is as follows:

- Reduction in reject parts: 10% of hardware cost
- Reduction in processing cost: 3% of hardware cost
- Net reduction: 13% of manufacturing cost

An example of cost savings for specific missile systems is given below. Conservative figures were used in obtaining the data (i.e., lower production rates and low MLB costs).

SYSTEM	SYS/YR	MLB SAVINGS
Pershing	36	$ 10,062.00
Dragon	6,000	58,500.00
Stinger	9,000	58,500.00
TOW	6,000	39,000.00
ATI	120	7,410.00
Chaparral	3,000	29,250.00
		$202,722.00

Additional savings would be realized if applied to other missile systems.

ASSUMPTIONS

The stated benefits assume that a production machine will be developed capable of processing 120 8" x 10" printed circuit boards per hour.

UPGRADING AND STANDARDIZATION OF PRINTED WIRING BOARD MATERIAL AND RELATED SPECIFICATIONS

J. R. Kubik

Hughes Aircraft Company
Fullerton, California 92634

SYSTEM/PANEL AREA/COMPONENT

Various/Test Equipment/Printed Circuits

PROBLEM

Primary and secondary documents applying to printed wiring boards that are imposed by the military require upgrading and standardization in order to provide more meaningful coverage at a reduced cost. Although good basic specifications have been written that cover most aspects of printed wiring boards, they require changes that would not only enhance their value, but result in better standardization and uniformity in design and manufacturing.

PROPOSED SOLUTION

A considerable amount of work has been done in the form of industry surveys relating to current documentation requirements. This work was performed under government contract and identifies many areas where changes would be beneficial. These changes would be in the form of refinements to existing requirements and the inclusion of coverage for items not presently mentioned such as ancillary materials for staking, thermoconductivity, potting, thermal mounting plates, flexible board systems, polyimide materials and microdevices. There is also a need for standardization among military specifications regarding design allowables, use of type RA fluxes, solder fitting of interfacial holes and guidelines as to the use of pliant buffer materials on glass components. An overall program is proposed to identify specific specification problems and recommend solutions.

PROJECT COST AND DURATION

Estimated costs are as follows:

Engineering Review		$80,000.00
Documentation		80,000.00
	Total	$160,000.00

The estimated duration of the program would be 24 months.

BENEFITS

This program would provide more reliable printed circuit boards at a reduced cost.

It is anticipated that a 2% savings in circuit board costs would be realized. An example of cost savings for specific missile systems is given below. Production rates and PCB costs used in the calculation are considered conservative.

SYSTEM	SYS/YR	PCB SAVINGS	MLB SAVINGS	TOTAL SAVINGS
Pershing	36	$ 8,370.00	$1,548.00	$9,918.00
Dragon	6,000	39,600.00	9,000.00	48,600.00
Stinger	9,000	48,600.00	9,000.00	57,600.00
TOW	6,000	39,600.00	6,000.00	45,600.00
ATI	120	6,120.00	1,140.00	7,260.00
Chaparral	3,000	25,200.00	4,500.00	29,700.00
				$198,678.00

Further savings would be realized if applied to other missile systems.

ASSUMPTIONS

It is assumed that an overall cost savings of 2% in subsequent production would be realized through successful completion of this program.

HEAT PIPES FOR CIRCUIT CARDS

Dr. K. S. Sekhon

Hughes Aircraft Company
Fullerton, California 92634

SYSTEM/PANEL AREA/COMPONENT

Various/Test Equipment/Environmental Control.

PROBLEM

Current and future advances in high power density microcircuits such as computer memories, high power transistors, LSI wafers and other high performance integrated circuits will necessitate the use of sophisticated, but inexpensive cooling techniques. The circuit card heat pipe, already developed by Hughes-Fullerton, can meet the current and future cooling requirement for high power density components. It can handle power levels three to five times greater than those of existing cooling techniques and still maintain uniform temperature over the entire card. This circuit card heat pipe can be used whenever circuit card power densities exceed the limitations of conventional convection and conduction cooling techniques. Weight and space savings will result from consolidation of the electrical components from several conventional cards onto a single high power density card with heat pipe.

Standard heat pipes for circuit cards have been developed and small batch quantities have been manufactured. However, there is a gap between the present prototype production and mass production to be cost effective. The present manufacturing method costs $400 per heat pipe which makes production economically unattractive. Manufacturing methods can be optimized to reduce this cost significantly to approximately $40 per heat pipe.

PROPOSED SOLUTION

The purpose of this project will be to establish quantity production techniques for circuit card heat pipes. Significant system cost reductions will result when production quantities of the circuit card heat pipes are manufactured. To reduce manufacturing cost, primary emphasis will be placed on the following items:

- Establish a wick attachment technique to replace the costly spot welding used for prototype fabrication.
- Establish a low cost shell stamping technique to replace the chemical milling operation used for prototype fabrication.
- Establish a shell bonding technique suitable for quantity production.

- Establish a vacuum/fill station for the accurate dispensing of small quantities of heat pipe fluid to at least ten heat pipes at one time.

- Establish a test station for circuit card heat pipe performance verification under dynamic conditions.

- Execute a short production run to verify established procedures.

- Provide data for fabrication specifications.

This project will reduce the cost of manufacturing heat pipes for circuit cards from $400 to $40 for each unit.

PROJECT COST AND DURATION

Pilot Equipment Design	$100,000
Pilot Equipment Fabrication	30,000
Pilot Equipment Installation	5,000
Pilot Production and Technical Data	5,000
Total	$140,000

Estimated duration of the project is 12 months.

BENEFITS

The objective of this project is to make available techniques, procedures and data for the quantity production of low cost, light weight, high thermal efficiency circuit card heat pipes. This project is essential to establish manufacturing methods and data to meet the requirements of current and future high power density electronic systems.

The application of circuit card heat pipes is not limited to one type of system, but can be used whenever high power density and high packaging density circuit cards are required. This project would result in a significant increase in production rates and cost reduction. The current prototype manufacturing cost is $400/unit. With the establishment of mass production engineering techniques characterized above, the manufacturing cost in high volume is estimated at $40/unit or a 90% cost reduction.

ASSUMPTIONS

The stated benefits assume that a circuit card heat pipe production facility would be established and optimized. It is also assumed that the production rate would be at least 250 units per month.

CONTINUOUS MONITOR SYSTEM

Joint Industry/Army Conference on Missile Manufacturing Technology Test Equipment Panel.

INTRODUCTION

This paper addresses itself to one of the problems of mass production of sophisticated hardware: The problem of continuous monitoring of the manufacturing process for the assessment of the final product. The Continuous Monitor System enables the vast amount of digital data generated during the production cycle of a product to be recorded and stored for quality assurance and failure analysis.

The proposed equipment does not address itself to any one manufacturing process or any missile system in particular. It is proposed as a capability which will enable new production methods to be utilized by monitoring the production process so that ordnance can be manufactured and stored, confident that it will perform to specification when called upon.

Problem Definition and Proposed Solution

Prior to the advent of the high density digital recorder, it was not practical to simultaneously use large numbers of high resolution sensors because the amount of digital data generated was too much for the on-line computers to handle, and the amount of magnetic tape required to store the data for off-line analysis became unwieldy.

The Continuous Monitor System became a viable product with the advent of the high density digital recorder. The high density digital recorder will store data at a packing density of 800 kilobits to the inch. At this packing density, it is possible to monitor 100 high resolution sensors for 8 hours or 3000 high resolution sensors for 20 minutes. Whereas this represents the maximum capability of the Continuous Monitor System, a typical system is likely to monitor 100 channels of 200 Hz data for 8 hours with a 1% resolution, or 50 channels of the same data for 8 hours with a 0.1% resolution. Another example is 100 channels of 5 kHz data monitored for 20 minutes with a resolution of 0.1% or the same data monitored for 40 minutes with a 1% resoltuion. From the above, it can be seen that the Continuous Monitor System has considerable flexibility in its application.

Comparison with Conventional Methods

An example of present monitor methods is taken from the production of solid propellants. Production of this material is monitored and due to the high frequency nature of the data, the data is recorded in analog format on magnetic tape or with light sensitive paper. The Continuous Monitor System is able to digitize these high frequency components and record them in digital format for computer analysis.

The Continuous Monitor System records the data on magnetic tape. This enables the data to be rapidly located and analyzed in a different time frame from that at which it was recorded. As an example, 8 hours of production monitoring can be analyzed in 20 minutes and the data can be easily and permanently stored for failure analysis, should the need arise.

A second example of how the Continuous Monitor System can reduce missile cost is that of the recording and analysis of data taken from the final checkout of a missile within its silo. The Continuous Monitor System will enable 1000 or more parameters to be simultaneously monitored and data analyzed in a faster or slower time frame at the discretion of the

equipment officer. The Continuous Monitor System can also be used to program the checkout of the installation with the checkout sequence recorded on the high density digital recorder and the acceptance limits stored along with the checkout sequence for comparison with the measured parameter.

Project Cost and Duration

The following estimated costs are for two (2) basic configurations: The first, Item A, will provide for continuous monitoring of 50 high resolution sensors; the second, Item B, will provide for the simultaneous monitoring of 1000 sensors:

Item A

Description	Qty	Cost/Unit	Cost/Total
Tape Transports	2	$25,670	$51,340
Record Electronics	1 lot	15,000	15,000
Digital Sig Input	1 lot	2,500	2,500
Output Filters	1 lot	1,000	1,000
System Engineering		NRE	50,000
Documentation		NRE	INC
Installation & Checkout		NRE	INC
Total			$119,840

Item B

Description	Qty	Cost/Unit	Cost/Total
Tape Transport	1	$29,980	$29,980
Record Electronics	1 lot	30,000	30,000
Digital Sig Input	1 lot	30,000	30,000
System Engineering		NRE	75,000
Documentation		NRE	INC
Installation & Checkout		NRE	INC
Total			$164,980

The estimated duration of the project is 240 days.

COMPANY NAME

Bell & Howell
Datatape Division

PARTICIPANT'S NAME, ADDRESS AND PHONE

Anthony G. Fairfield
300 Sierra Madre Villa
Pasadena, California 91109
213-796-9381

Title: Improved Microcircuit Reliability with reduced total cost by using High Temperature Operating Tests (HTOT).

System/panel: area/component: ALL MISSILES/Guidance and Control/Microcircuits

Problem: The many manufacturing and performance advantages of using microcircuits are compromised due to either device reliability problems or the high cost of processing reliable devices. Both manufacturing and maintenance costs are increased due to unreliable microcircuits.

Proposed solution: Microcircuit costs reflect material, labor and yield losses. The major cost factors are created by the yield losses that occur after the labor intensive assembly and test activities. The solution is to use HTOT testing techniques early in the microcircuit manufacturing cycle. If successful substantial device cost reductions should be possible.

Project cost: Estimated costs are as follows:

Demonstration Experiment	$600,000
Engineering Services for Microcircuit Manufacturer Help and Facility Design	250,000
Total	$850,000

Benefits: The benefits to be derived from this project are a reduction in recurring hardware costs and a substantial improvement in device reliability. The cost reductions are as follows:

INITIAL CONDITIONS:
Yield Baseline As Follows:

Linear Chips	- 30%
Linear Packaged Product	- 6.67%
Digital Chips	- 42%
Digital Packaged Product	- 40%

Cost: Chips Linear $.14 each
Digital $.07 each

HTOT $100 per wafer

Assembly & Test

Linear $1.65 each
Digital $1.11 each

SAVINGS:

FINAL YIELD	% SAVINGS DIGITAL	% SAVINGS LINEAR
20%	-	49
40%	-	75
60%	7	83
80%	30	87
99%	44	90

Assumptions: Microcircuit final yields will improve due to early HTOT testing as follows:

Digital:	75 to 95% Yield
Linear:	40 to 75% Yield

McDonnell Douglas Astronautics Company - East

Mr. Mort Stitch
Dept. E-261
Box 516
St. Louis, Missouri 63166
(314) 232-6662